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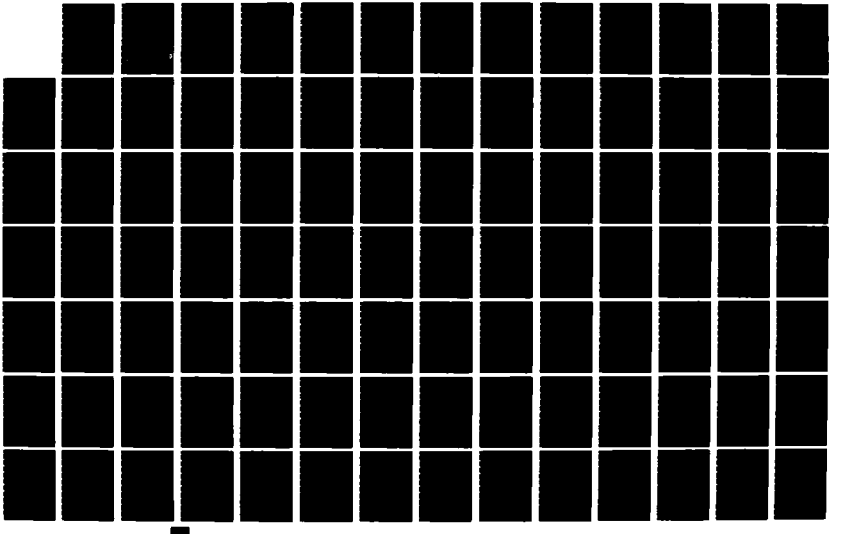

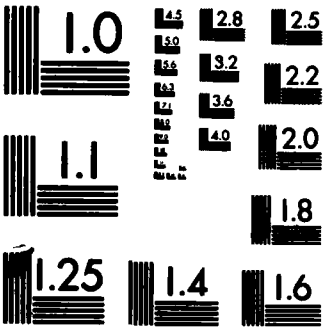

AN
AUTOMATIC SINE-WAVE GRATING CONTROLLER
TO BE USED FOR
CONTRAST SENSITIVITY TESTING

THESIS

AFIT/GE/EE/83D-65 Mark H. Swann
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DEPARTMENT OF THE AIR FORCE
AIR UNIVERSITY (ATC)
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Wright-Patterson Air Force Base, Ohio

AFIT/GE/EE/83D-65

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Approved for public release; distribution unlimited

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THESIS

Presented to the Faculty of the School of Engineering

of the Air Force Institute of Technology

Air University

in Partial Fulfillment of the

Requirements for the Degree of

Master of Science in Electrical Engineering

by

Mark H. Swann, B.S.E.E.

GS-12 USAF

Graduate Electrical Engineering

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PREFACE

The Air Force Aerospace Medical Research Laboratory (AFAMRL), Wright-Patterson AFB, Ohio, is developing a new test for the human visual system. This new test determines the subject's contrast sensitivity by viewing different levels of contrast of a sine-wave grating displayed on a video monitor. Since brightness and contrast levels of the sine-wave grating might vary undesirably during a test session, AFAMRL is interested in having an automatic level adjustment device so that a high reliability of the vision tests may be obtained.

This thesis is the fourth effort in developing an automatic brightness and contrast device which can be used to insure the test parameter standards of the vision tests. The first thesis analyzed the basic concept of such a controller and proposed a general design approach. Specific hardware for constructing the proposed controller was also ordered but arrived too late to be built. The second thesis effort used the original design and equipment to build a prototype controller. Although the hardware was built and the software was written in this second attempt, there was not enough time for either to be tested.

A third effort was made to produce a controller for automatically adjusting brightness and contrast. An extensive amount of redesign of both the hardware and software provided the new controller with a broader range of spatial frequency operation and a much more user-friendly

means of operation.

This thesis utilizes the new controller design and completes the unfinished sub-systems to make an operational contrast sensitivity vision test controller.

I would like to express my sincere appreciation to Major Arthur Ginsburg, Aviation Vision Laboratory, AFAMRL, as the sponsor for this thesis.

My appreciation also extends to the support members of the Signal Processing Laboratory for their continued technical assistance throughout this thesis effort: Mr. Robert Durham, Mr. Dan Zambon, Capt. Lee Baker, Mr. Orville Wright, and Mr. Richard Wager.

A special appreciation goes to Dr. Matthew Kabrisky for being my thesis advisor during this project, and for his invaluable help and guidance in the design, construction, and testing of this thesis effort.

My most sincere appreciation goes to my wife, Jean, for all the assistance and encouragement she provided while this thesis was being developed and written.

Mark H. Swann

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ABSTRACT

This report documents the additional design, construction, and testing of a brightness and contrast controller system which includes an embedded microcomputer. It is planned that researchers will use this controller to maintain prescribed video output of laboratory video monitors during vision research.

The controller requires a video signal consisting of a sine-wave grating. A 512-element photodiode array directly measures the monitor's screen to produce an analog signal which is then digitized and stored in the computer. These data are used to compute the actual brightness and contrast of the monitor. Correction values are sent to the brightness and contrast control circuits when the desired and measured values differ.

In an attempt to complete the controller's system requirements, the controller prototype hardware was completed and partially packaged. Closed-loop system testing was performed for both the brightness and contrast control circuitry. Brightness and contrast control circuitry, a vertical synch pulse generator, a user-interface console, and power supply with additional voltage-regulator circuitry were designed and added to the existing prototype. Existing software was tested and modified to allow the controller to operate more accurately. Final packaging and with additional system testing, must be accomplished for the controller to be a finished product.

I INTRODUCTION

BACKGROUND

Extensive research is being conducted in the area of measuring the human visual response. Even though the standard eyechart is effective in measuring ultimate visual acuity by testing one's ability to see small, high contrast letters and symbols under bright light (ideal conditions), it does not correctly evaluate the subject's ability to detect or distinguish objects under many operational conditions. Such conditions for an aircraft pilot might include detecting or recognizing a target during unfavorable conditions of visibility. Identifying a target under hazy (low contrast) and/or low-light conditions are examples (Ref 1:4).

The Air Force Aerospace Medical Research Laboratory (AFAMRL) at Wright-Patterson AFB, Ohio, is currently studying new ways of measuring an individual's visual response over a range of spatial frequencies. One test approach involves measuring a subject's contrast sensitivity to sine-wave gratings presented on a cathode ray tube (CRT) over a range of spatial frequencies, but at a fixed orientation (Ref 1:6).

To an observer, a sine-wave grating appears like a group of fuzzy bars. It is defined as "a repeated sequence of light and dark bars that has a luminous profile which varies sinusoidally, about a mean luminance, with distance" (Ref 1:6). It is estimated that this pattern best

emulates a uniform representation of varying contrast for simulating objects to be detected in realistic situations (Ref 1:19).

In one test approach to measure a subject's contrast sensitivity, AFAMRL uses an Optronix sine-wave grating generator, controlled by a Rockwell AIM-65 test system, to create a sine-wave grating on a video monitor. The microprocessor-controlled signal generator/test system inputs the sine-wave grating to the monitor at different spatial frequencies while varying the level of contrast and/or brightness. When the subject just detects a pattern on the monitor, he presses a button which signals the system to record the brightness and contrast values. The test system then sets a different spatial frequency and changes the contrast-adjust slew rate. From the series of measurements, AFAMRL is able to determine the subject's contrast sensitivity over a range of spatial frequencies.

In another test approach, an optical signal generator is manually adjusted to create the sine-wave grating on the monitor. A subject views the monitor at a preset brightness and adjusts the contrast of the grating until the bars are just at the threshold of becoming undetectable. The test is then repeated for several more bar widths so that a contrast sensitivity can be calculated (Ref 1:19).

A problem with the current tests is that brightness and contrast of the test pattern are calibrated only before the test session. Any additional calibration checks made during

the test could be annoying to the subject and cause the test results to be inaccurate. Researchers are concerned that the brightness and contrast signal levels input to the monitor might not always be the same as those output by the monitor because of line voltage variations and calibration drift. Experimental data gathered during these tests could therefore be less than accurate and induce errors in determining the subject's contrast sensitivity (Refs 1:8 and 2:103). AFAMRL has asked that a device be designed and constructed that will monitor and control the brightness and contrast levels of the test patterns as they are being used during a contrast sensitivity test.

In 1980, Capt. Kenneth Martindale began development of a brightness and contrast controller as an AFIT thesis project. Martindale designed a controller based on a Z80 microprocessor, a Reticon photodiode array, and Datel analog-to-digital (A/D) and digital-to-analog (D/A) converters in his thesis project. After reviewing his design, AFAMRL was satisfied with the preliminary design and ordered the hardware needed to build the proposed controller. The equipment arrived too late for Capt. Martindale to begin construction of a working model (Ref 3:3).

Capt. Albert Lawson resumed development of Martindale's controller in 1981. Lawson used Martindale's design and built most of the hardware for the controller. He also developed several Z80 assembly language programs to operate the controller. Because of the amount of software which was

needed, along with the large amount of hardware circuitry wiring required, Lawson was not able to finish development of the controller in the time alloted (Ref 4:2).

Capt. Barry Baxley continued the development and implementation of the controller in 1982 as a thesis project. After a detailed analysis of the original controller design, Capt. Baxley determined that the Martindale-Lawson controller would have to be redesigned (Ref 5:6). Most of the hardware and software in Baxley's new design was constructed and tested in his thesis project, but because of the extensive amount of redesign, he was not able to complete the development and implementation as originally planned (Ref 5:43-48).

PROBLEM STATEMENT

The object of the original thesis was to develop a system capable of controlling brightness and contrast of a sine-wave grating on a video monitor. Due to Baxley's thorough analysis and extensive redesign of the Martindale-Lawson controller, the basic problem of this thesis is to complete the development and construction, and to verify correct operation of the new test-pattern controller.

SCOPE

Because of the complexity of the hardware and software required in controlling sine-wave gratings being displayed on a visual monitor, it was not possible to complete the

complete development of the controller as originally planned. Upon development and construction of the additional necessary circuits, the controller was tested as a complete double-feedback loop, automatically adjusting both brightness and contrast. The software operating the controller during these tests was that which was designed by Baxley. Tests were later conducted using the software which was modified in this thesis.

A lens and Reticon array position arrangement was set up to correctly project the visual pattern displayed by the monitor onto the photodiodes. The center vertical section of the monitor was the part of the display being sampled.

Although not extensively tested with the system, a newly designed software program was written to more accurately use the Reticon array values in calculating an actual brightness and contrast output from the monitor. Specific reasons why this software revision is needed will be detailed in Chapter IV.

ASSUMPTIONS

This thesis was based on several assumptions with regard to the hardware and software used. They are as follows:

1) The Reticon hardware was assumed to provide analog voltages proportional to the light intensity present on each of the Reticon array's photodiodes.

2) It was assumed that output "drift" on each of the photodiodes would be an undetectably minute amount and would

not change with time. Although adjustable in the Reticon circuitry, the drift would be considered as nonexistent so that continuous recalibration would not be required.

3) Consistency in output signals for all photodiodes when given a uniform light input was assumed. This consistency would require the sensitivity of the photodiodes to be within a few percent of each other.

4) Finally, it was assumed that Baxley's evaluation and redesign of the controller circuit and software were correct and did not require any in-depth reevaluation. All of the circuitry which he constructed on breadboards were assumed to follow the schematic diagrams as drawn in his thesis.

GENERAL APPROACH

This project was divided into three main phases: existing system analysis, circuitry construction, and system testing. Existing system analysis was the first step in evaluating what circuitry had been constructed and the design parameters that had been set forth. The construction phase included analyzing the suggested design recommendations contained in Baxley's thesis, constructing the circuitry and testing those sub-systems. After each sub-system was constructed and tested individually, it was then incorporated into the total system for testing.

The five areas (sub-systems) in which circuitry additional to that already constructed was designed are:

1) Reticon/Lens Test Mount Apparatus - required to project the monitor's visual image onto the photodiode array.

2) Brightness Control Circuitry - required by the Z80 microprocessor to control the brightness (luminance) of the video monitor.

3) Contrast Control Circuitry - required by the Z80 microprocessor to control the contrast of the sine-wave grating.

4) Vertical Synchronization Pulse Generator - required by the existing scan-start pulse generator (SSPG) to synchronize the vertical synch pulses of the monitor with the Reticon clock to produce a start pulse for the Reticon circuits.

5) User-Interface Control Console - control console used by the system operator to adjust desired brightness, desired contrast, and system reset.

After designing and constructing the sub-systems, the controller software was tested. It was not until the total system was tested that it seemed necessary to make modifications to the existing controller software. Baxley had provided a complete software program which proved to be well designed, even though modifications seemed necessary after testing the total system with the feedback loops operational.

The sub-system circuits were breadboarded and debugged. The user-interface control console was designed, built, and tested as a part of the total system. Finally, actual test

evaluations were made to determine the applicability of a sine-wave grating controller.

SEQUENCE OF PRESENTATION

The remaining chapters of this thesis provide a detailed presentation of what was accomplished in this thesis and recommendations on what must be completed before a working sine-wave grating controller can be fully operational. Chapter II provides a description of the sub-system hardware which was constructed along with a general existing hardware description. In Chapter III, sub-system hardware design, construction, and testing is described, along with those circuit parameters used in the design stages. Controller software is described in Chapter IV by stating the controller system requirement along with the previous approach and modifications which are necessary for correct system operation. System operation is presented in Chapter V, and finally, Chapter VI presents final conclusions and recommendations.

II CONTROLLER HARDWARE

SYSTEM DESCRIPTION

Figure II-1 depicts the controller as a whole system with each sub-system as integrated together. An Optronix generator sends a video signal to a monitor, where a sine-wave grating is produced. A Reticon photodiode array, mounted in front of the monitor's screen, and its associated sampling circuits scan the monitor and produce an analog signal representing the luminance detected on each of the array's 512 photodiodes. This string of samples is

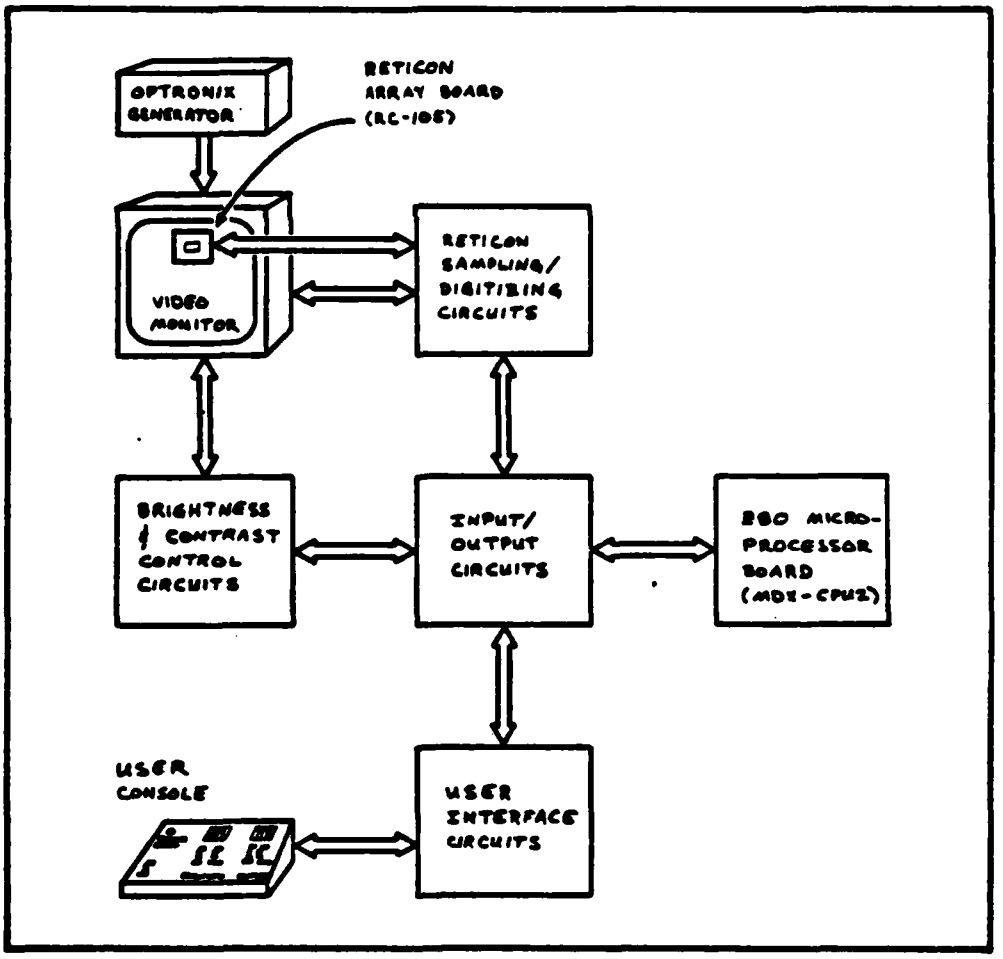

Figure II-1. Controller -- Total System (Ref 5:16)

digitized and sent to the Z80 processor via the input/output (I/O) circuits.

The system console allows the user to reset the system to preset values for desired brightness and contrast or to set new values. Preset values are determined by the settings on switches S5 and S6 of the internal controller circuitry. New desired brightness and/or desired contrast values are input via the switches on the user-interface control console.

The Z80 analyzes the Reticon data and computes the actual brightness and contrast present on the video monitor. These values are compared with saved values for desired brightness and contrast. If the desired and actual values differ, corrections are then sent to the control circuits which readjust the monitor's brightness and contrast.

Each of the circuits shown in Figure II-1 is described in more detail in the following sections.

RETICON SAMPLING AND DIGITIZING CIRCUITRY

Figure II-2 depicts a functional diagram of the Reticon sampling/digitizing circuit. As previously described, the Optronix generator produces a sine-wave grating on the video monitor's screen. The vertical synch pulse generator (VSPG) produces vertical synch pulses which trigger the scan start-pulse generator (SSPG). The SSPG synchronizes the synch pulses with the Reticon clock to produce a start pulse for the Reticon circuits. The SSPG also provides the user an adjustable delay so that the time at which a scan of the

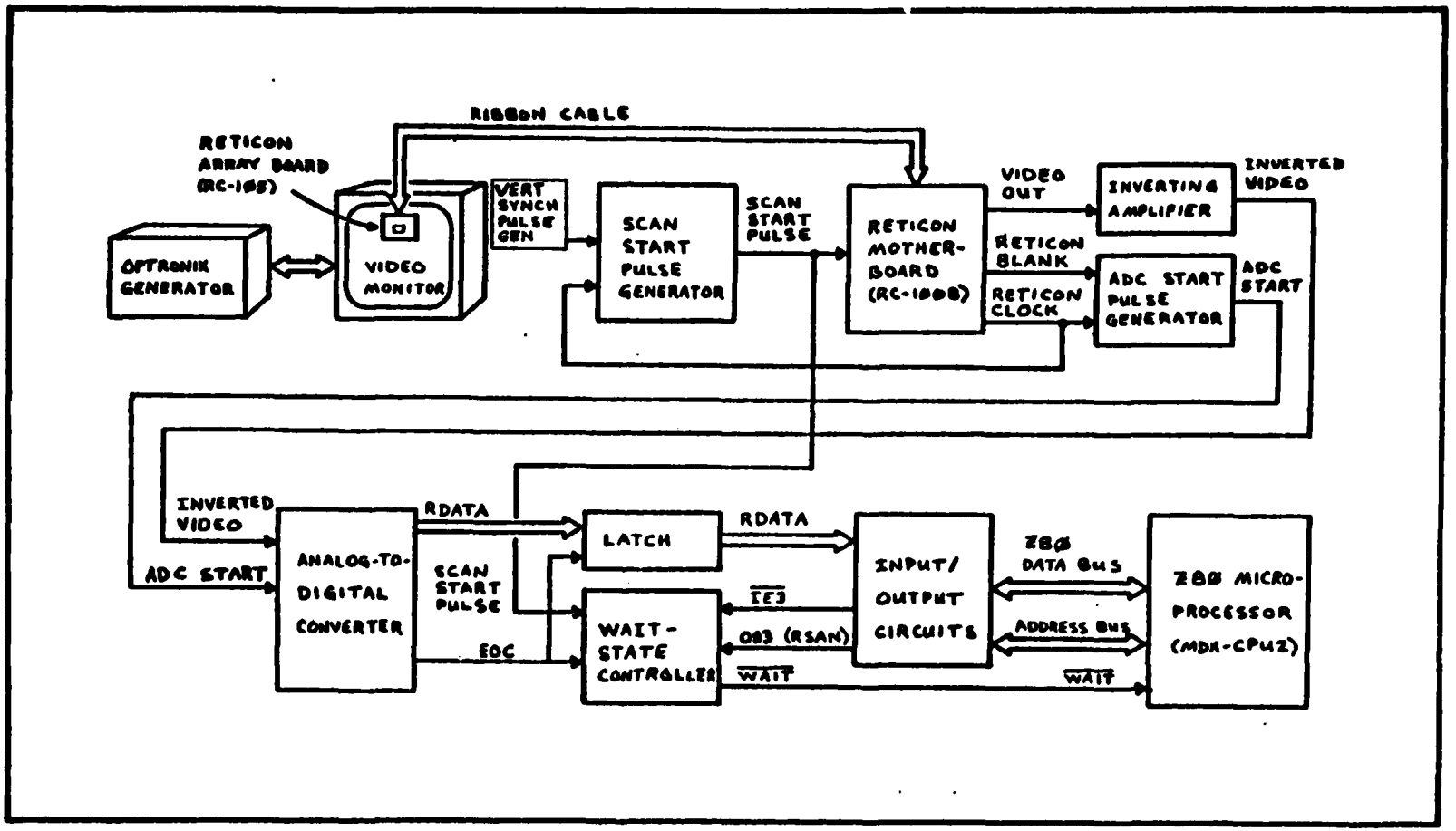

Figure II-2. Reticon Sampling and Digitizing Circuit (Ref 5:18)

monitor's screen is to start can be set. Thus, the SSPG synchronizes the Reticon sampling circuit with the VSPG's vertical synch pulse so that the electron beam of the video monitor does not trace across the Reticon array. A more detailed explanation of the vertical synch pulse generator appears in Chapter III.

The Reticon circuits are divided into two boards -- a standard "motherboard" which contains most of the circuitry, and a small "array board" which contains only those components which must be located close to the array. The array board can be located up to 30 inches away from the motherboard and is mounted behind a lens in front of the video monitor's screen. The Reticon circuits scan the monitor and produce a string of 512 samples when triggered by the start pulse. Each sample's voltage is proportional to the light detected by the corresponding photodiode on the Reticon array and appear as a sampled and held boxcar video signal at the video output of the Reticon motherboard when viewing a sine-wave grating.

The video out signal is then inverted by the inverting amplifier for digitization by the analog-to-digital converter (A/D) circuit. This inversion is necessary because the Reticon video output is a 0 to -5 volt analog signal and the A/D converter used accepts inputs in the 0 to +5 volt range. The inverting amplifier also provides gain-adjustment for the Reticon video signal. This feature will be used when calibrating the controller for specific light-intensity levels.

The A/D converter start pulse generator uses the Reticon clock and blanking outputs to determine when each new Reticon sample is ready to be digitized.

The A/D's end-of-conversion (EOC) pulse strobes an 8-bit latch after each conversion is complete. This stores the new value for input to the Reticon data port (RDPORT) while the A/D circuit digitizes the next sample. The EOC pulse also signals the wait-state controller (WSC) that a new sample has been digitized.

The wait-state controller provides synchronization between the Reticon scanning/digitizing circuits and the Z80 microprocessor. The WSC synchronizes the Z80's attempts to read a new video scan with the actual start of the next scan. Vertical synch pulses from the vertical synch pulse generator trigger the Reticon scan. The WSC then synchronizes the Z80 with the Reticon circuits. This circuit also forces the processor to wait until each new sample is ready to be read at the RDPORT.

MOSTEK MPX-CPU2

The Z80 microprocessor board, which is the heart of the controller, is a Mostek MDX-CPU2. All of the overhead functions of the controller are performed by the the Z80. Brightness samples from the Reticon sampling and digitizing circuits are read in through the I/O ports. Calculations are made using the data from these samples to determine actual brightness and contrast values for the grating on the

video monitor. The actual values are compared with desired values and, if needed, correction signals are sent to the control circuits. The Z80 also updates desired values for brightness and contrast when the user signals that desired values are to be updated. This is done through the use of the update switches located on the user-interface console. The desired values are then scaled by the Z80 for proper comparison with actual values. Detailed descriptions of the software routines which perform these functions are listed in Baxley's thesis (Ref 5:20-23) and summarized in Chapter IV of this thesis.

INPUT/OUTPUT CIRCUITRY

An interface between the Z80 microprocessor and the rest of the sine-wave grating controller system is provided by the I/O circuits. As shown in Figure II-3, the I/O is composed of an address decoding circuit, a data bus buffer, four input ports, and three output ports. Address decoding for a fourth output port is provided, although a fourth output port is not required for the current system design.

The address decoder selects the appropriate input or output port when the processor attempts to read from or write to one of the seven ports used. The decoder also controls the direction of data flow in the data bus buffer, depending on whether the Z80 is attempting to read or write data. The buffer generally is set for passing data from the Z80 data bus to the ports at all times, except when the decoder detects that the processor is trying to read one of

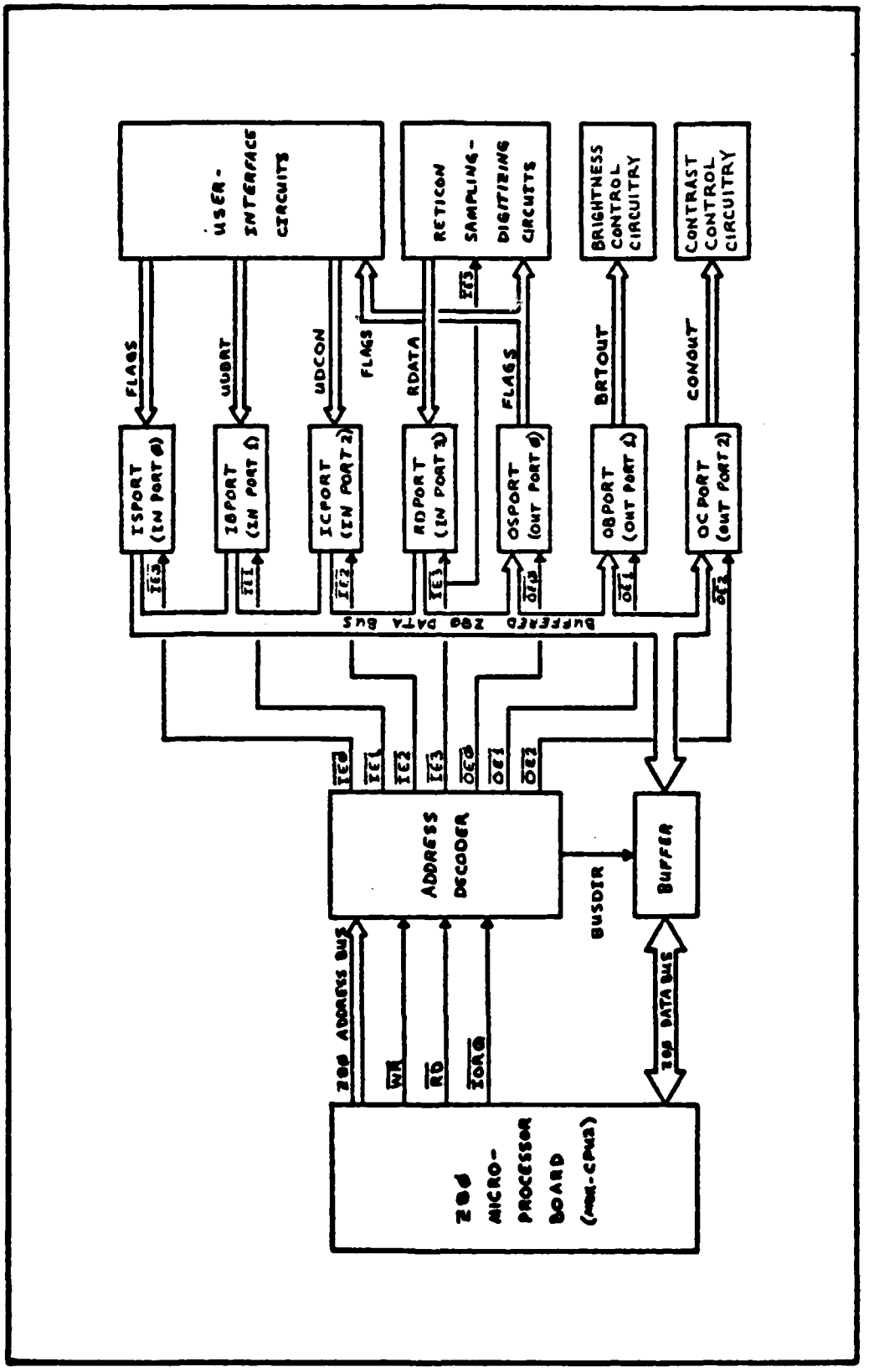

Figure II-3. Input/Output Circuits (Ref 5:21)

the four input ports.

The buffer is provided to minimize electrical loading of the Z80 data bus. Due to fan-in, fan-out, and capacitive loading considerations, there are limits on the number of devices which can be tied to the data bus. The buffer allows several ports to be connectd to the bus while placing only a single load on it. Because the current controller design places only seven ports on the data bus, the buffer could probably be omitted. The buffer was provided, however, in case additional ports were added later.

The seven ports include the following:

1) Input port 0 is the input status port, ISPORT. It is used to input various status-related flags to the processor. At present, only bits 0 and 1 are used. Bit 0 (IS0) is the brightness update flag (BUFLG) which signals that the user wishes to update the stored value for desired brightness. Bit 1 (IS1) is the contrast update flag (CUFLG) that similarly indicates desired contrast is to be updated.

2) Input port 1 is the input brightness port, IBPORT. This port passes the 8-bit binary-coded decimal (BCD) value for unscaled desired brightness (UDBRT) from the user-interface circuits to the Z80.

3) Input port 2 is the input contrast port, ICPORT. It is used to pass the 8-bit BCD value for unscaled desired contrast (UDCON) from the user-interface circuits to the processor.

4) Input port 3 is the Reticon data port, RDPORT. This port sends the Reticon samples from the Reticon

sampling and digitizing circuits to the processor.

5) Output port 0 is the output status port, OSPORT. The Z80 sends control signals to the external hardware through this port. At present, only bits 0, 1, 2, and 3 are used. Bit 0 (OS0) is the brightness flag clear (BFCLR) bit which resets the brightness flags, brightness update flag (BUFLG) and brightness not-updated flag (BNUFLG), after desired brightness has been updated. Similarly, Bit 1 (OS1) is the contrast flag clear (CFCLR) bit which resets the contrast flags, contrast update flag (CUFLG) and contrast not-updated flag (CNUFLG), after desired contrast has been updated. Bit 2 (OS2) is the preset bit used to initialize the system to default values for desired brightness and contrast when the system first comes up or is reset. Bit 3 (OS3) is the Reticon scan (RSCAN) bit used by the Z80 to reset the wait-state controller.

6) Output port 1 is the output brightness port (OBPORT). It sends brightness output (BRTOUT) values to the brightness control circuit to correct errors detected in the monitor's luminance.

7) Output port 2 is the output contrast port (OCPORT). It sends contrast output (CONOUT) values to the contrast control circuit when corrections in the monitor's contrast are needed.

BRIGHTNESS AND CONTRAST CONTROL CIRCUITRY

The brightness and contrast control circuits are another set of important sub-systems of the controller. Baxley provided two output ports in his design and hardware circuitry for sending an 8-bit control word (BRTOUT) to the brightness control circuit and an 8-bit control word (CONOUT) to the contrast control circuit. As shown in Figure II-4, these circuits send control signals to the video monitor so that the video monitor's output display will adjust to the new brightness and contrast.

The brightness control circuit consists of digital-to-analog (D/A) converter and monitor brightness driver circuitry. The D/A converter circuitry converts the 8-bit control word (BRTOUT) to an analog voltage which ranges from 0.0 volts-dc (vdc), where all 8 bits are zero, to +10 vdc, where all bits are ones. This 39 millivolt per bit voltage controls the monitor brightness driver circuitry which replaces the brightness control potentiometer of the monitor. The driver circuitry contains an operational amplifier (op-amp) and a transistor circuit which convert the 0-to-10 volts from the D/A converter to a bias grid control voltage adjustment. This grid voltage adjusts the brightness of the picture tube for a range of approximately 0 to 36 foot-Lamberts (fL).

Similarly, the contrast control circuit consists of digital-to-analog (D/A) converter and monitor contrast driver circuitry. The D/A converter circuitry converts the 8-bit control word (CONOUT) from the microprocessor to the

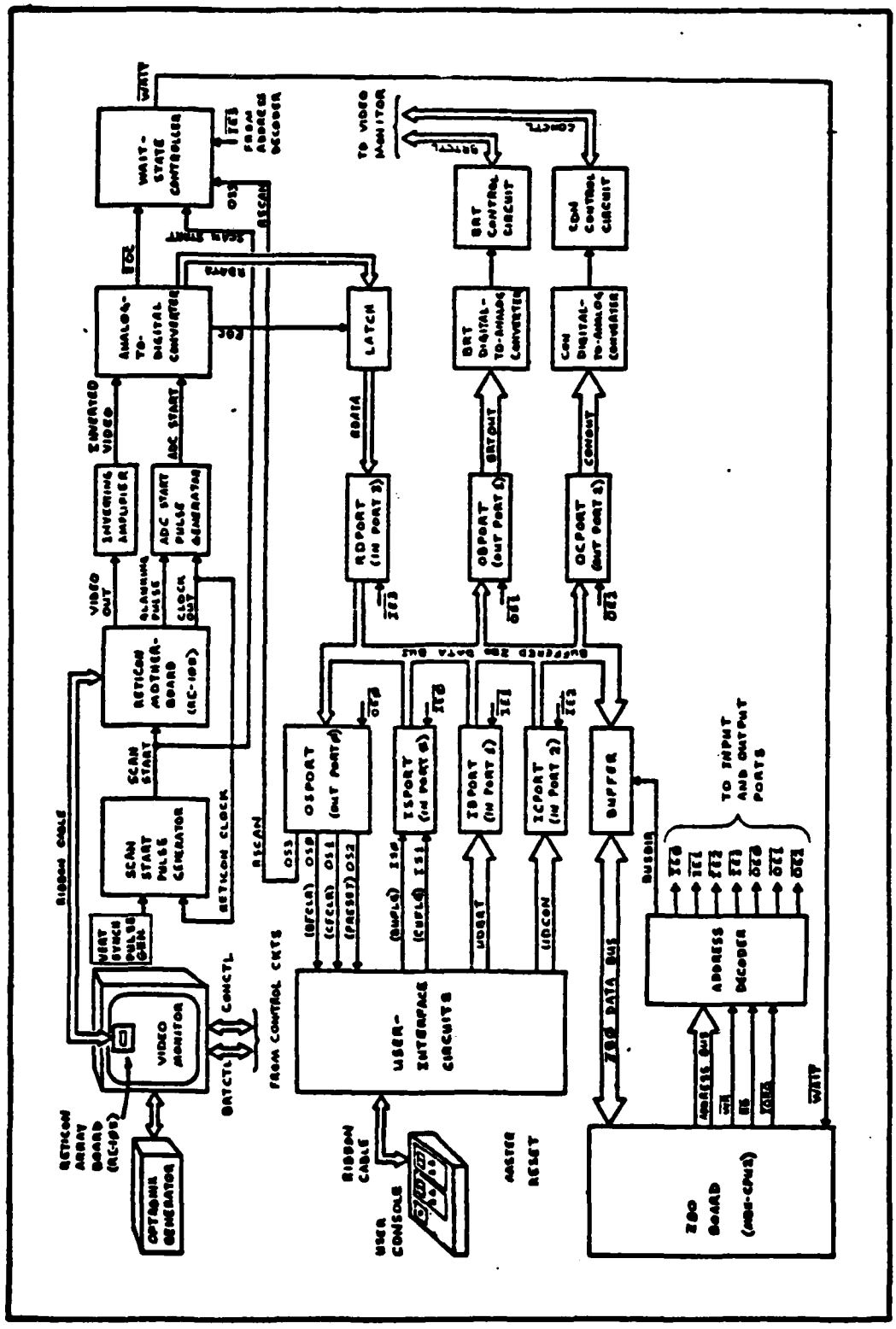

Figure II-4. Controller System Functional Diagram (Ref 5:27)

0-to-10 volt analog voltage in steps of 39 millivolts. This voltage is routed to an operational amplifier and associated circuitry which converts the voltage into a video amplifier control signal for the luminance processor. The output of the video amplifier is connected to the wiper of the monitor's contrast potentiometer. Only the video amplifier of the luminance processor was needed to control the monitor's contrast. The design, construction, and testing of these circuits are explained in detail in Chapter III.

USER-INTERFACE CIRCUITRY

A functional diagram of the user-interface circuitry is included as Figure II-5, showing various components and interconnections. Switches on the user console are used to input the control setting and updating of desired values for brightness and contrast. A contact bounce eliminator is used to debounce these switches. Outputs from the switch debouncer drive a dual-rate clock circuit, counter select logic, and flag circuitry.

Whenever switch S1 or S2 is toggled, the dual-rate clock (DRC) outputs a positive-going transistor-transistor-logic (TTL) pulse which is sent to the counter select logic for driving the desired brightness and contrast counters. When the switch is first toggled, the clock operates at approximately one cycle per second. If the switch is continued to be held either up or down, the clock automatically switches to a faster rate, 4 Hz, after four clock cycles. The clock then stops and resets as soon as

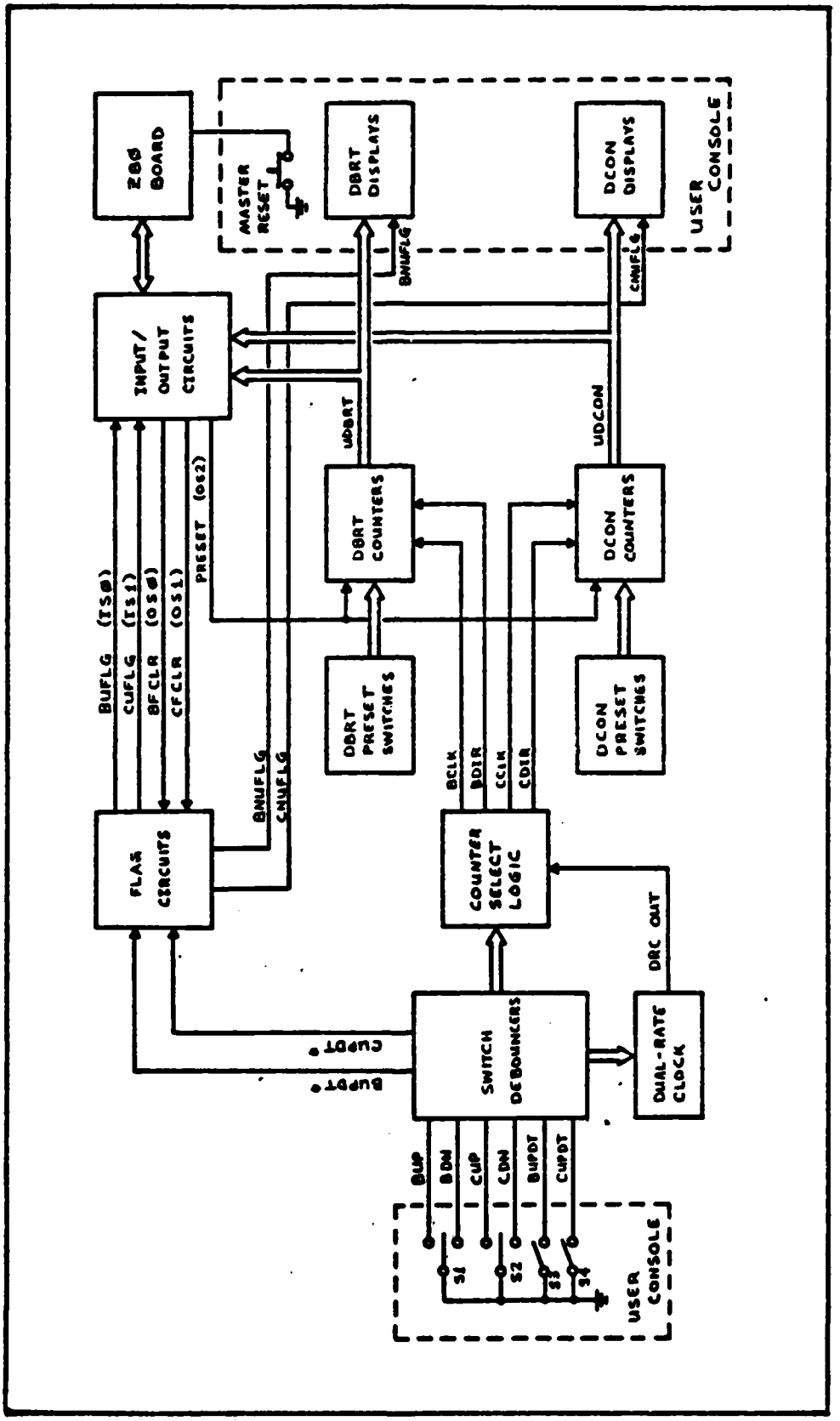

Figure II-5. User-Interface Functional Diagram (Ref 5:24)

the activating switch (S1 or S2) is released. Outputs from the switch debouncers and the dual-rate clock serve as inputs to the counter select logic which increments or decrements the brightness and contrast counters, depending on which switch is activated and whether the switch is toggled up or down.

The brightness and contrast counters send the brightness and contrast values that have been selected to the appropiate I/O input ports and to the displays at the user-interface console. The counters also have inputs which provide preset default values for the counters whenever the controller is initialized by the power on/off switch. These inputs are preset by setting the desired brightness (DBRT) and desired contrast (DCON) preset switches, S5 and S6.

The user-interface circuitry also utilizes flag circuits to signal the operator when a brightness or contrast value has been changed but not updated. This circuitry is also used to signal the Z80 that a new brightness and/or contrast value is to be updated. Finally, the I/O circuits interface the user-interface circuitry with the Z80 central processing unit (CPU).

SUMMARY

This chapter described first the controller as a whole system with each sub-system as integrated together, and then each of the five sub-systems as an independent system. The next chapter will describe the specific design, construction, and testing aspects of the controller

circuitry developed in this thesis.

III HARDWARE DESIGN, CONSTRUCTION, AND TESTING

This chapter outlines and describes in detail subsystems and associated circuitry that was designed, constructed, and tested in this thesis.

RETICON ARRAY MOUNT DESIGN

After spending the first few weeks of this thesis project analyzing the work Baxley had performed in his thesis, a suitable mounting configuration was sought for the Reticon photodiode array. In his design, Baxley had recommended that the array be mounted directly on the video monitor's screen (Ref 5:16). By using a black-and-white video camera focused on a sine-wave grating pattern (Ref 2:133-134), different mounting locations on the screen were tried in order to find the most efficient location for the array to be mounted. By monitoring the Reticon video out signal with an oscilloscope with the amplitude set at 1 volt/division and the time base set at 50 microseconds/division, it could be seen that the Reticon array could not accurately detect the video displayed on the monitor. It was decided that one reason for this was that the half-inch Reticon photodiode array, resembling a dual-in-line-pin integrated circuit (DIP), is packaged such that the photodiodes are a significant distance away from the outer clear-glass window. Another reason for the inaccuracy was that the phosphor coating of the video monitor's picture tube is even a greater distance inside the outer glass

envelope. These two details prevented the Reticon array from measuring fine details of the image on the phosphor.

In order to measure appropriate details of the display produced by the grating generator, a 25.4-millimeter (1-inch) focal length lens was used to focus a sharp image of the monitor screen directly onto the 512 elements of the Reticon array. Black, flexible, high-pressure hose, 2.5 inches in diameter, was used to build a prototype mount for the lens and Reticon array board. With this apparatus, it was possible to adjust focus of the video image onto the photodiode array by monitoring the video out signal from the Reticon circuitry.

While testing this mounting structure, two problems became evident. First, by sampling only a small portion of the video monitor's screen (.5 inches), there would thus be a limit on the sine-wave grating used as to the number of cycles per degree (cpd) and size of the cycle. This would directly restrain the sine-wave grating patterns used by AMRL and the controller would therefore be of small utility in research. The second reason was found to be related to the amount of brightness output by the monitor at different locations on the screen. Martindale tested a similar video monitor for uniform brightness output and recorded differences found with respect to location on the screen (Ref 3:33-35). Considering these things, another mounting configuration was sought.

After taking into consideration that a subject views a

large portion of the video monitor when being tested for contrast sensitivity, it was decided that a more realistic approach in designing a Reticon array mount would be to focus a representation of the whole screen on the photodiode array. Since the photodiode array consists of 512x1 photodiodes, a vertical slice of the monitor's video output of a horizontally displayed sine-wave grating would be more realistic. Dr. Matthew Kabrisky, thesis advisor, supplied a 1-inch focal length, adjustable aperture lens, taken from a video camera, for use in this design. An all-purpose mounting apparatus with three-axis adjustments was incorporated in the lens setup. The apparatus was ideally suited for mounting the Reticon array board. Equations for calculating the distances required for projecting the 8.5-inch vertical screen onto a 0.5-inch vertically mounted photodiode array, using a 1-inch focal length lens, are shown below:

$$1/F = 1/O + 1/I \quad (1)$$

$$L1/L2 = O/I \quad (2)$$

where: F = focal length of the lens
O = object distance from the lens
I = image distance from the lens
L1 = object size
L2 = image size

By setting F = 1.0 inches, L1 = 8.5 inches, and L2 = 0.5 inches in equations (1) and (2), it was calculated that the lens should be set 18 inches away from the CRT screen (O=18 inches), and the photodiode array should be set 1.058 inches away from the focal point of the lens (I=1.058 inches). Approximate distances were set on the workbench

since the three-axis mount could adjust the focus with great accuracy directly on the array.

Figure III-1 shows the physical layout of the Reticon array mounted on the three-axis mount, lens, and video monitor. This mounting arrangement was used throughout the rest of this thesis.

For the controller to have flexibility and portability, a portable housing with the lens and three-axis mount needs to be fabricated. The Reticon array, mounted on the three-axis mount, could be adjusted, up and down, left and right, and focused back and forth, as long as the lens-to-monitor screen remained at the calculated 18 inches. Distances other than this would cause the photodiode array to "see" either less than the full vertical slice or more than the vertical slice. Less than the full vertical slice would not cause any forseen errors, but more than the vertical slice of the monitor would include the border and housing of the video monitor, thereby producing great errors in calculating brightness and contrast.

This mounting arrangement was used throughout the rest of this thesis for projecting the video image onto the photodiode array. Due to the requirement for other circuitry to be designed and tested, this Reticon array and lens mount were not packaged into a portable unit as needed.

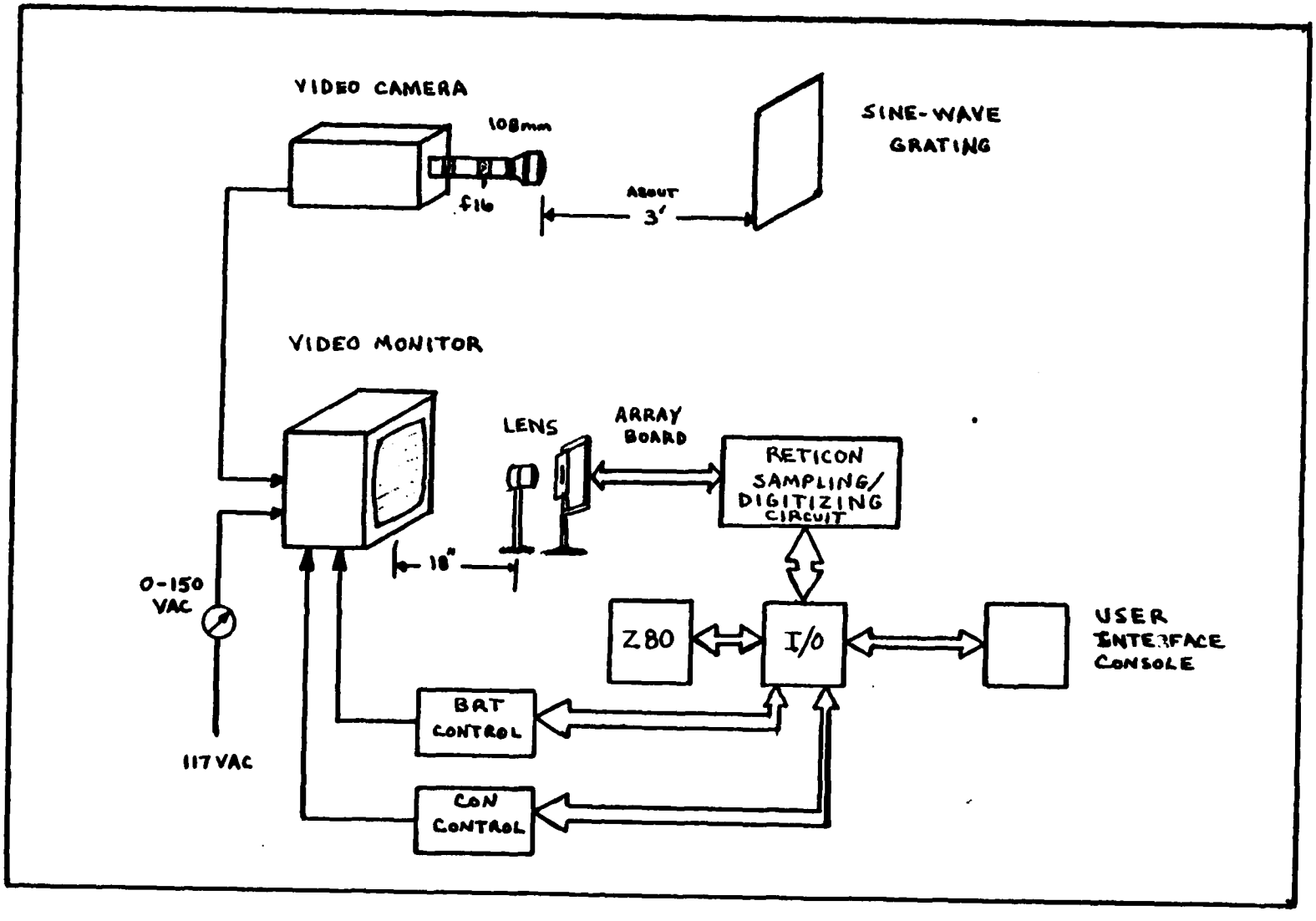

Figure III-1. Test System Setup

BRIGHTNESS CONTROL CIRCUITRY

An important sub-system of the controller is the brightness control. As mentioned in Baxley's thesis, Martindale (Ref 3:6-10, 22-25) had bench-tested a brightness control amplifier for regulating the brightness of the video monitor, and Lawson (Ref 4:9) had constructed a digital-to-analog converter for controlling the amplifier (Ref 5:26, 74).

D/A Converter Circuit

Since Lawson had previously found that a Datel DAC-UP8BM digital-to-analog converter was a satisfactory device to be used as a converter, a circuit was constructed using the recommended application notes in Datel's Engineering Product Handbook. After building this circuit, using a DAC-UP8BM found on Lawson's wire-wrap board, it was tested and found to be inoperative. While trouble-shooting the circuit, the DAC-UP8BM was found to be bad. The possibility of obtaining another one for this circuit, as well as a second one to be used in the contrast control circuit, was checked on. The Datel factory was contacted for an estimation on the amount of time it would take for them to fill an order once they received it. Although their response was one to two weeks, it was four weeks before the two new D/A converters were received.

While waiting for the D/A converters, another similar D/A converter was found readily available in the AFIT Digital Lab. A D/A circuit was built by using an Analog

Devices AD561J, 10-bit monolithic D/A converter and by following the recommended circuit construction provided in the Analog Devices Manual for a unipolar 0 to +10 volt output. Only the eight most significant bits were used. (See Appendix B.)

This circuit was first tested by including a DIP switch containing eight individual rocker switches and an eight-resistor network DIP chip. Using a digital multimeter to monitor the output, the D/A circuit was zero-adjusted by inputing zeros for all eight bits, and then adjusted for a +10 volt upper limit by inputing ones for all eight bits by the DIP switch. Each successive bit-count resulted in a 39-millivolt analog output increase.

Control Amplifier

The brightness control amplifier was designed and built next. By analyzing the video monitor's brightness circuit, it was decided that a transistor drive circuit could replace the brightness potentiometer (500-Ohm, 10-turn).

An oscilloscope was used to measure the signal characteristics at the grid (pin 2) of the video monitor picture tube. The 24 volt pulse peak-to-peak signal varied from a +44 to +20 volt peak-to-peak signal (brightness potentiometer fully clockwise) to a -14 to -40 volt peak-to-peak signal (brightness potentiometer fully counterclockwise). At the brightness potentiometer wiper, connection 21, the 3 volt signal varied from +40 volts

(fully clockwise) to -18 volts (fully counterclockwise).

A suitable transistor with VBE of about 60 volts, hfe of about 100, and a low current drive requirement was found as a replacement for the brightness potentiometer. Figure III-2 shows the 2N2102 as wired in a test circuit to determine the voltage requirement for operating the transistor as a potentiometer replacement.

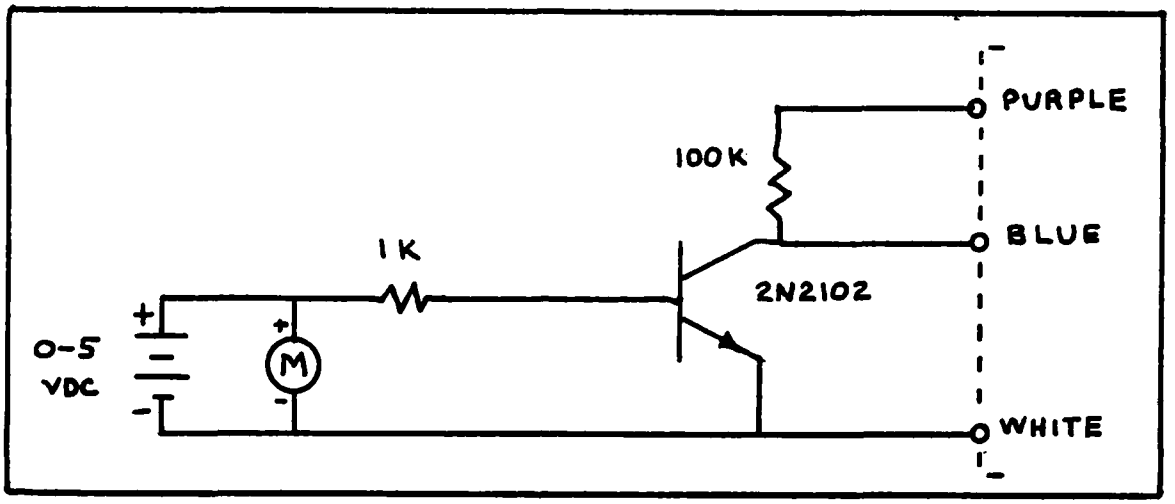

Figure III-2. Brightness Potentiometer Test Circuit

This transistor circuit was tested by using a variable voltage supply to determine what input voltages were necessary for adjusting the video monitor's brightness from minimum to maximum. It was found that an input of +1.95 vdc was minimum brightness and +0.4 vdc was maximum brightness.

Subsequently, circuitry that would convert the 0-to-10 volt D/A converter output to a voltage suitable for driving the transistor circuit input, 1.95 to 0.4 vdc, was designed and built. This circuitry consisted of an LM741 operational-amplifier (op-amp) connected as a dc-biased

inverter along with several resistors and trimpots. This circuit linearly converted the D/A converter's 0-10 vdc (00000000 to 11111111) to a +1.95-to- +0.4 vdc transistor drive circuit voltage. U27 of Baxley's hardware circuitry (Ref 5:72) was connected to the eight inputs of the brightness control D/A converter by a 10-conductor ribbon cable. Testing of the brightness portion of the controller is now ready to be undertaken.

Testing

The completed brightness control circuit was tested by substituting the monitor's brightness control potentiometer with the three output wires from the control amplifier and measuring the light output from the monitor. Before the monitor's potentiometer was removed, this manual brightness control adjusted the video monitor's luminance from about 0 foot-Lamberts (fL) to about 36 fL. This was measured with a Spectra Pritchard Photometer, Model 1980A-PL, aimed at the center of the monitor's screen about eight feet away with no ambient room light. The brightness control circuit was then connected and tested using the photometer. Table C-1 (see Appendix C) is a list of the data and Figure III-3 is a plot of the data obtained by sequencing through the six most significant bits of the D/A converter by inputting zeros and ones on the DIP switch.

Another set of data was also obtained after adjusting the brightness control amplifier potentiometer to obtain a

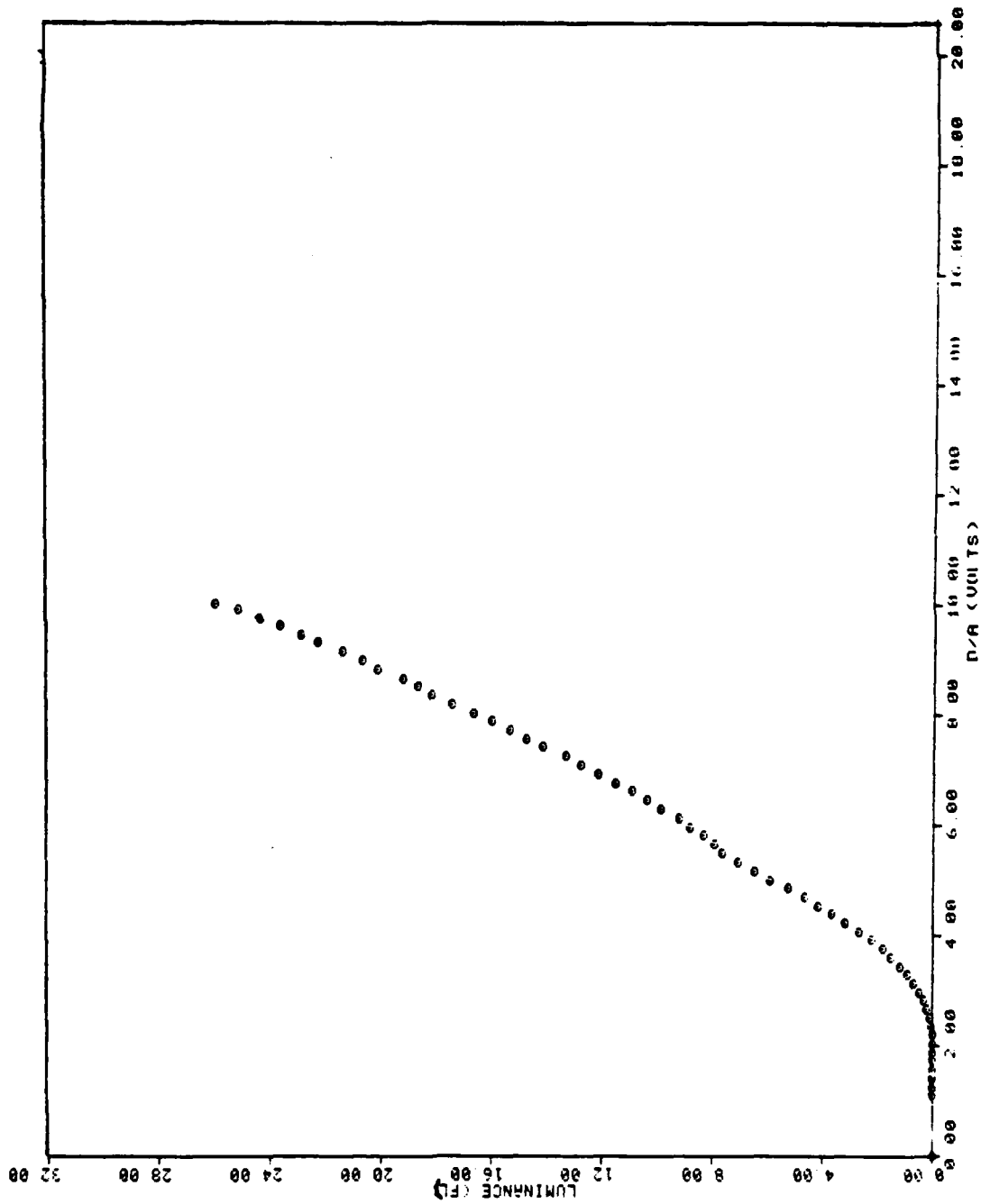

Figure III-3. Luminance vs. D/A Output Voltage - 1

maximum output of approximately 36 fL. This adjustment was made to directly correspond with the brightness output obtained with the original monitor potentiometer. Table C-2 and Figure III-4 display this second set of data recorded after making the adjustment. No other adjustments of the brightness control circuit were made following those described above.

A series of tests were made with the controller sensing and automatically adjusting the video monitor's brightness level. With the video camera functioning as a signal generator by being focused on a sine-wave grating and the monitor's contrast potentiometer set at 50 percent, the brightness closed-loop response was tested. The system held a consistent brightness level with values of approximately 10-15 fL input at the user-interface console. Higher brightness levels caused the controller to loop-oscillate, gradually increasing brightness to maximum, then immediately outputting minimum brightness, increasing gradually to maximum, etc. Values lower than the 10-15 fL range caused the brightness loop to oscillate by decreasing the brightness to minimum, outputting maximum brightness and adjusting to minimum again, etc. This was caused by the Reticon sampling a value that was calculated by the Z80 to be too low and the Z80 then incrementing a higher value of brightness output to the D/A converter. If the Reticon continues to sample a value too low for the Z80, the Z80 will continue to increase the digital output until an all high output (11111111) is sent. If the Z80 increments the

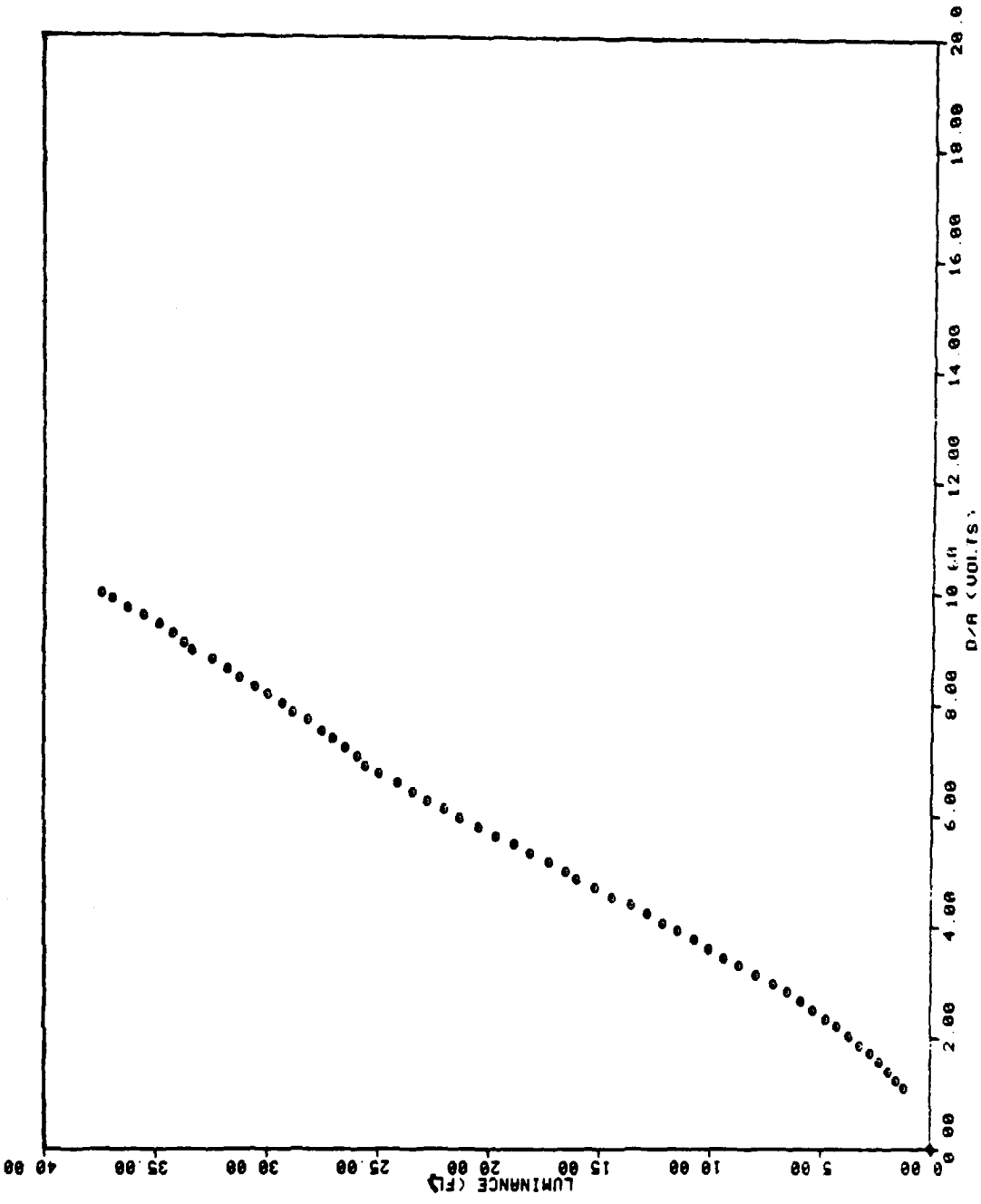

Figure III-4. Luminance vs. D/A Output Voltage - 2

output one bit higher, all lows are output 11111111 +00000001 = 00000000) to the D/A converter, which will cause a minimum output of brightness. The pattern is also similar when the desired value is lower than the actual value (when already minimum) of the monitor. This, decrementing the minimum 8-bit word when at the minimum (00000000 - 00000001 = 11111111) also causes the wrap-around oscillation. This problem and a suggested solution are addressed in Chapter IV.

With the system adjusted for a stable feedback with desired brightness set at 12 fL, several test trials were performed to simulate the real occurrence possibility of line-voltage fluctuations. The system monitor was plugged into an autotransformer which had an adjustable ac voltage output. With the brightness feedback loop operating stably at 117 vac into the monitor, the autotransformer was readjusted to 125 vac and 110 vac. The brightness feedback loop successfully made corrections to the brightness control of the monitor and the video brightness output remained constant. The schematic diagram of the completed brightness control circuitry is illustrated in Figure III-5.

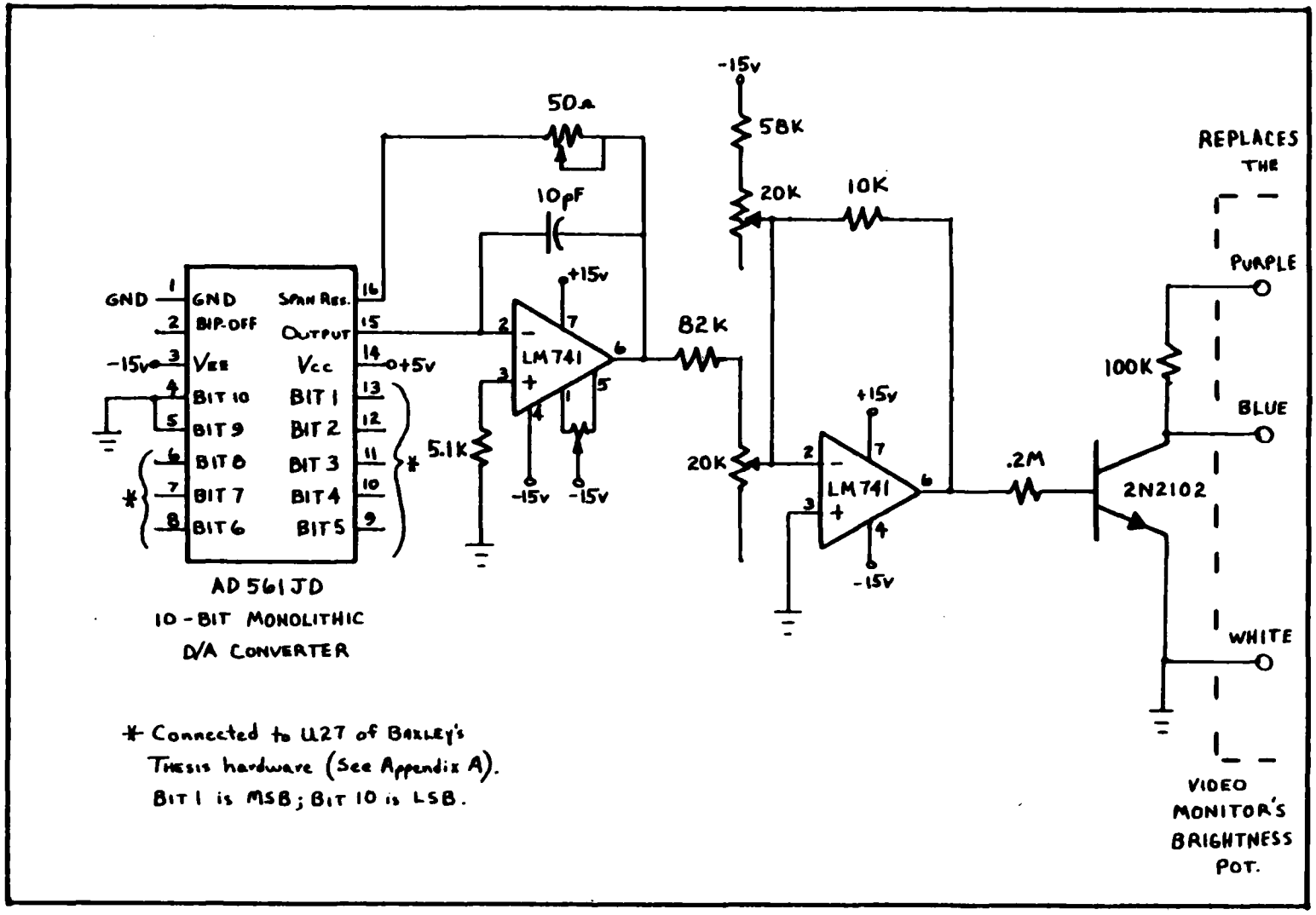

Figure III-5. Brightness Control Circuitry

CONTRAST CONTROL CIRCUITRY

Another important sub-system required for the controller to be a fully operational system is the contrast control circuitry. It was suggested by Martindale and Lawson that a luminance processor integrated circuit, ECG985, be used as the heart of the contrast control circuitry (Refs 3:6 and 4:29). According to Baxley, Martindale had bench-tested the luminance processor and was satisfied with its control over contrast (Ref 5:26).

D/A Converter Circuit

As mentioned earlier in this chapter, it had been originally planned to use the Datel DAC-UP8BM D/A converter for both the brightness and contrast control circuits. Due to the late arrival of this converter, an Analog Devices AD561J, 10-bit monolithic D/A converter was used to convert the 8-bit word from the I/O circuits to an analog control voltage so that the video monitor's contrast might be adjusted. Appendix B contains the specifications of this D/A converter and factory-recommended circuit configuration for unipolar, 0-to- +10 vdc, output. The two least significant bits of this converter were tied to ground since only eight significant bits were needed.

The D/A converter circuit was built using the manufacturer's circuitry description with an 8-bit DIP switch and 8-resistor DIP network. After this was constructed, the converter circuit was adjusted at zero (all zeros input) and at maximum +10 vdc (all ones input). Each

successive binary increment increased the analog output by about 39 millivolts.

Control Amplifier

The luminance processor was breadboarded with other required circuitry components for brightness and contrast control as suggested by the RCA Technical Specifications Handbook for the CA3144G (see Appendix B). The luminance processor on hand was a Sylvania ECG985, and was completely interchangeable with an RCA CA3144G. Video from the Dage camera was connected to pin 1 of the processor through a 1 Kohm resistor; the output, pin 7, was connected to an oscilloscope for measurement purposes. Output from the processor was not obtained until it was realized that the video input level had to be voltage biased to a much higher level. A voltage divider circuit was applied to the input which then produced an output. Another modification was made to the test circuitry to make it usable on a +15 vdc supply rather than the recommended +30 vdc supply.

Since the output of the luminance processor is inverted, an inverting op-amp circuit using an LM741 op-amp was connected to pin 7 of the processor. The output of the op-amp was then connected to the video monitor. With a video pattern input to the camera, output on the video monitor was seen, but it had a "smeared" appearance. It was determined that the inverting op-amp circuitry with the LM741 with a limited bandwidth of 1 MHz should be replaced

with a higher bandwidth op-amp. An LM318 op-amp with a bandwidth rating of 15 MHz was used in place of the LM741. It was noticed that the LM318 operated at a high temperature and should possibly be replaced with an LM118 op-amp with the same electrical characteristics, but higher temperature tolerance.

By adjusting the 50 Kohm potentiometer contrast control of the luminance processor circuit, a comparison was made with the video monitor's own contrast control potentiometer. The control potentiometer of the video monitor had much more linear control of the monitor's contrast, plus the clearness of the unaltered video picture was apparent when routed straight to the monitor rather than through the luminance processor and inverter circuit. With these disadvantages taken into consideration, another contrast control design was planned.

By looking at the schematic diagram of the contrast control portion of the video monitor, it was decided that contrast control might be accomplished by replacing the contrast potentiometer with a control circuit as was done for brightness. If there was a video signal located on the monitor's contrast potentiometer, the video amplifier portion of the luminance processor could possibly be used to control contrast rather than having to inject blanking pulses when using the luminance processor totally.

An oscilloscope was used to measure the signal characteristics on the contrast potentiometer of the monitor. Pin 1 (black wire) of the potentiometer was found

to be ground; pin 2 (beige wire), which is the wiper of the potentiometer, varied from ground to a maximum of 4.4 volts peak-to-peak video signal with a +4.4 vdc offset; and pin 3 (brown wire) was the fixed-level signal input to the potentiometer.

Figure III-6 depicts the test circuit layout for using the luminance processor as a video amplifier to control contrast. The video input from the potentiometer (brown wire) is connected to the video input, pin 1, of the processor. The output of the processor, pin 4, is directly connected to the beige wire (contrast control video input to the monitor) which is now disconnected from the potentiometer. Pin 5, ground, is connected to the black wire (ground) of the potentiometer.

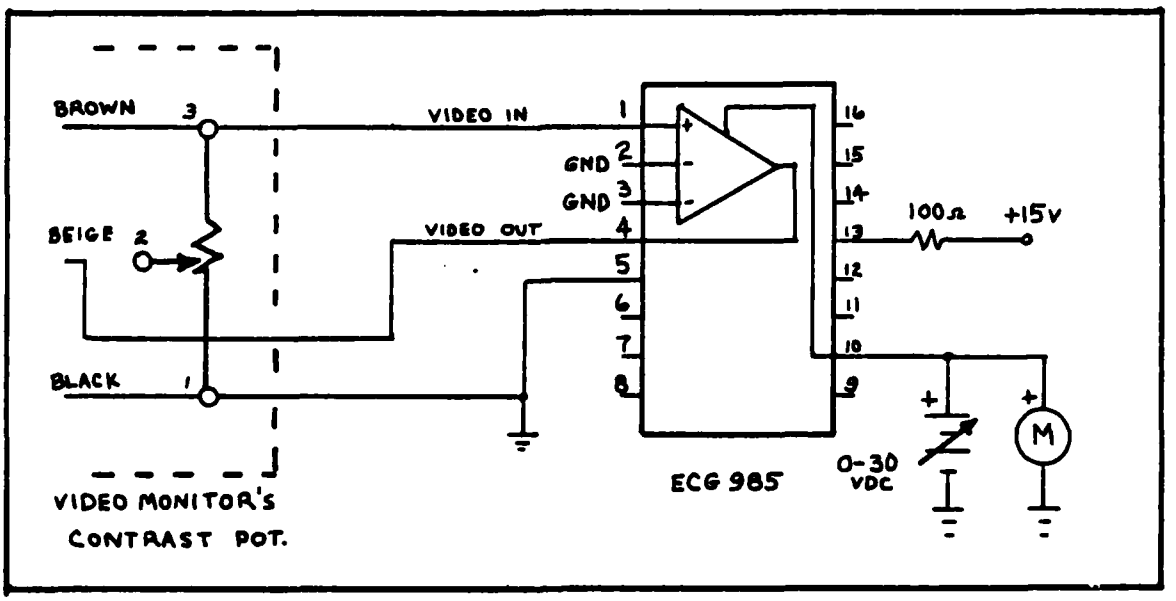

Figure III-6. Video Amplifier Test Circuit

After connecting this circuit to the video monitor as indicated, the control voltage input to the video amplifier was determined by connecting it to a variable voltage supply and by varying the voltage while monitoring contrast level. It was found that the control voltage required to fully adjust the contrast ranged from +12.2 vdc (minimum contrast) to +1.6 vdc (maximum contrast).

A circuit converting the 0-to- +10 vdc from the D/A converter to the +12.2-to- +1.6 vdc video amplifier control voltage was designed. It consisted of an LM741 op-amp set for inverting output with an adjustable dc offset. With the circuits connected together, the final contrast control circuit construction left was to connect the I/O contrast control output to the D/A converter input. U28 of Baxley's hardware circuitry (Ref 5:72) was connected by a 10-conductor ribbon cable to the eight inputs of the contrast control D/A converter. The completed circuitry schematic for the contrast control circuitry is illustrated in Figure III-7.

Testing

With the contrast control circuitry now constructed, testing of the control circuit was performed. The first set of tests tested only the contrast control loop by itself with the brightness control potentiometer back in the video monitor circuit. This would allow the contrast control to be tested without any brightness control feedback falsely altering the control function.

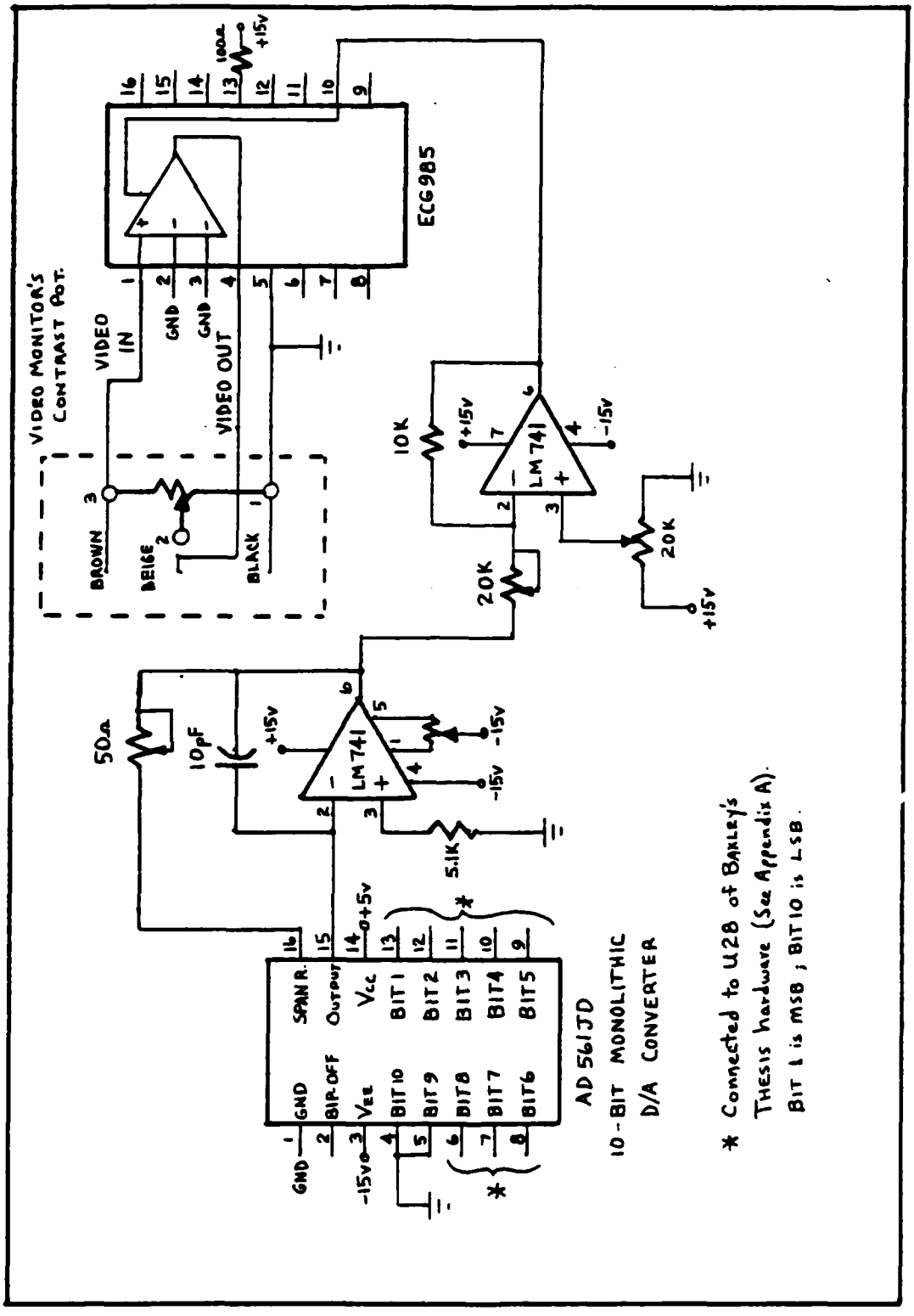

Figure III-7. Contrast Control Circuitry

The brightness potentiometer was manually adjusted to full clockwise, Wavetek set at 20 Hz, camera set at f16 and focused on the sine-wave grating with a one-bulb fluorescent fixture 12 inches from the grating, while the contrast setting was input on the user-interface console. Contrast automatically tracked and was stable for the contrast setting range of 20 to 40. This range appeared on the video monitor as varying from no visible contrast to a barely visible pattern. The brightness control potentiometer was then adjusted to a position three turns from full clockwise; when retested, contrast automatically adjusted and tracked from 20 to 40. With a contrast value of 47 input at the user-interface console, automatic tracking seemed to function properly while the brightness potentiometer was slowly adjusted over the full range. When the contrast was set for any setting greater than 47, oscillation of the contrast control began and was noticed as the pattern began bleeding across the screen with too much contrast. This then caused the contrast circuit to cycle from low to high, trying to increase the contrast to a higher limit as specified by the Z80. The wrap-around situation, as described in the brightness control section of this chapter, was also evident in the contrast control feedback loop.

Next, the brightness and contrast control circuits were both connected to the automatic control circuits for testing. It was found through a series of different brightness/contrast values input at the user-interface console that a stable output could be achieved at a value of

13/40. If any higher value for either brightness or contrast was input, the double-feedback loops would sometimes begin oscillation. Brightness values could be decreased while holding contrast constant, and contrast values could be decreased while holding brightness constant, but both varying over very much range together usually caused unrecoverable oscillation. The system would usually recover when set back to the 13/40 values.

Figure III-8 is a plot of the gain of the video amplifier inside the luminance processor. Data for this plot were obtained by inputting a 0-to- 4 volt peak, positive-going 15KHz pulse at pin 1 and monitoring pin 4 while sequencing the D/A converter control voltage from 00000000 (0 volts dc) to 11111111 (10 vdc). The plot depicts the linearity of the video amplifier used to replace the contrast potentiometer of the video monitor.

Further testing and calibration are yet required for the controller to operate over a complete range of brightness and contrast levels. Basic system construction and double-feedback loop testing have been accomplished so that design work may continue in a progressive and promising manner.

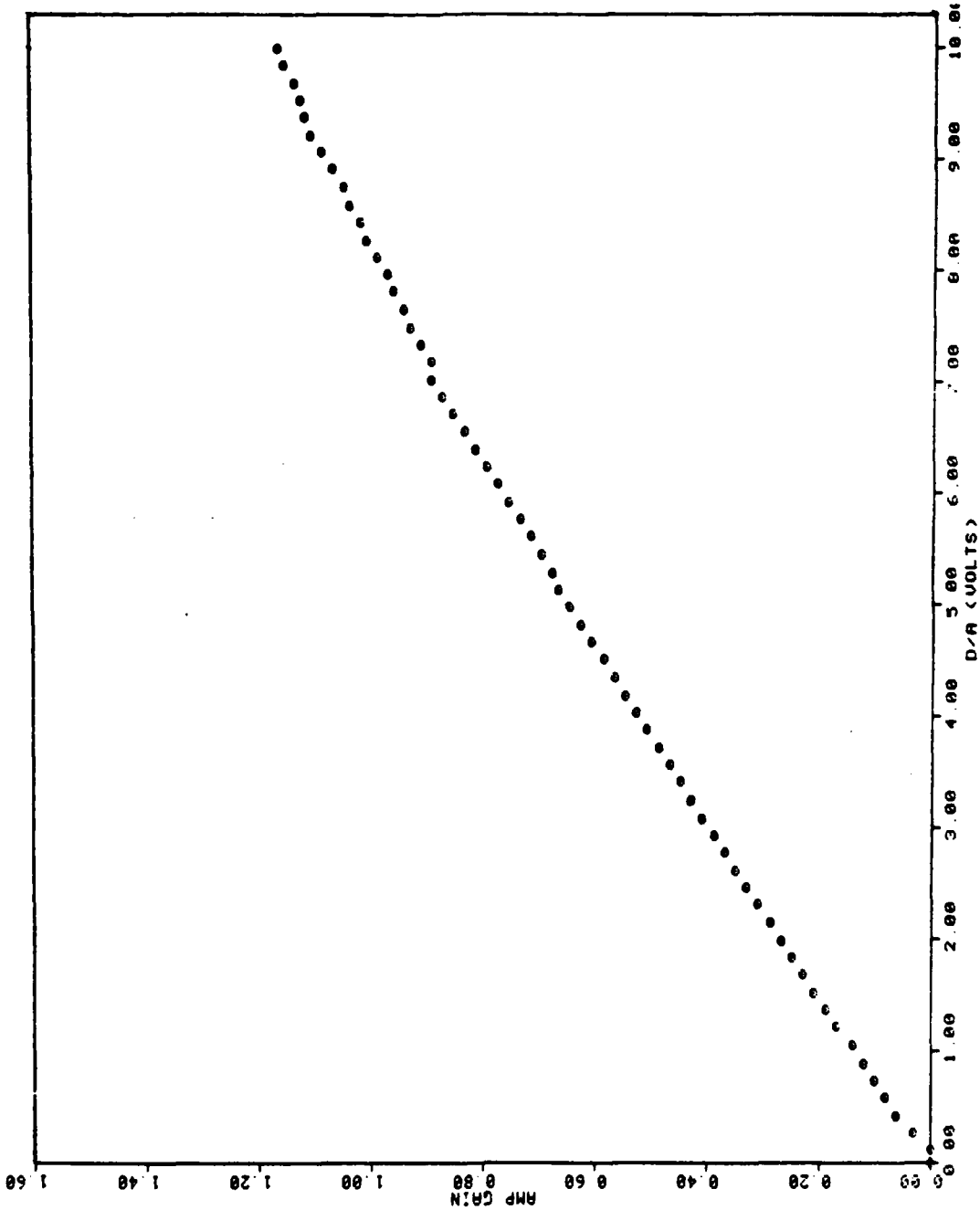

Figure III-8. Video Amplifier Gain Plot

VERTICAL SYNCH PULSE GENERATOR (VSPG)

While testing the controller with both the brightness and contrast control circuits operating automatically, a variable beat-frequency pulse was traveling through the Reticon video sample signal on the oscilloscope. This pulse was directly dependent on the Wavetek function generator that was supplying the vertical synchronization pulses for the scan-start pulse generator circuit (Ref 5:60). Baxley had used a frequency of 30 Hz in testing his basic sampling and digitizing circuitry. When the controller and Wavetek were first turned on, the Wavetek would require fine adjustments every few minutes to minimize this beat-frequency pulse on the samples output. It was also thought that this pulse disturbance would cause error-producing calculations each time the samples were read and brightness and contrast calculations were made from the sample data. Construction of a vertical synch pulse generator would be the only solution to this problem.

Design

Baxley had suggested that vertical synch pulses could be obtained from some circuitry point in the video monitor (Ref 5:17, 58). Rather than tap the vertical synch pulses from the monitor, it seemed more advantageous to design a circuit to generate the required pulses independent of the video monitor.

Since it had not yet been determined at what frequency the vertical synch pulse generator should operate, it was

decided that an even multiple of several frequencies be available. For the pulse generator to be independent of the monitor and yet utilize the same basis frequency, the pulse generator should derive its output from the 60 Hz ac line. This is the same source from which the video monitor and camera derive their vertical synch pulses.

Construction

Figure III-9 is the schematic diagram of the vertical synch pulse generator. Sixty Hz at 117 vac is taken from the line voltage and sent through a 0.1-amp fast-blow fuse, a 20-Kohm fixed resistor, and a 20-Kohm variable resistor. The wiper of the variable resistor taps a lower voltage ac signal which is then rectified through a diode. A load resistor and zener diode rated at 4.9 volts clips any excess voltage before the signal reaches the two 74LS14 inverters. These inverters shape the signal into a good TTL pulse before allowing it to become the clock input of the 74163 four-bit synchronous binary counter. The load of the counter is tied "high" so that the count sequence will continue as the clock continues to run. Outputs QA, QB, and QC are connected to a 74LS138 3-to-8 line decoder. This decoder converts the three-line binary input to a 1-in-8-line output. By using this counter and decoder together, a divide-by circuit is set up for a divide-by-2, divide-by-3, divide-by-4, and divide-by-5 circuit, selectable by a set of DIP switches. The output of the DIP switch is tied to the

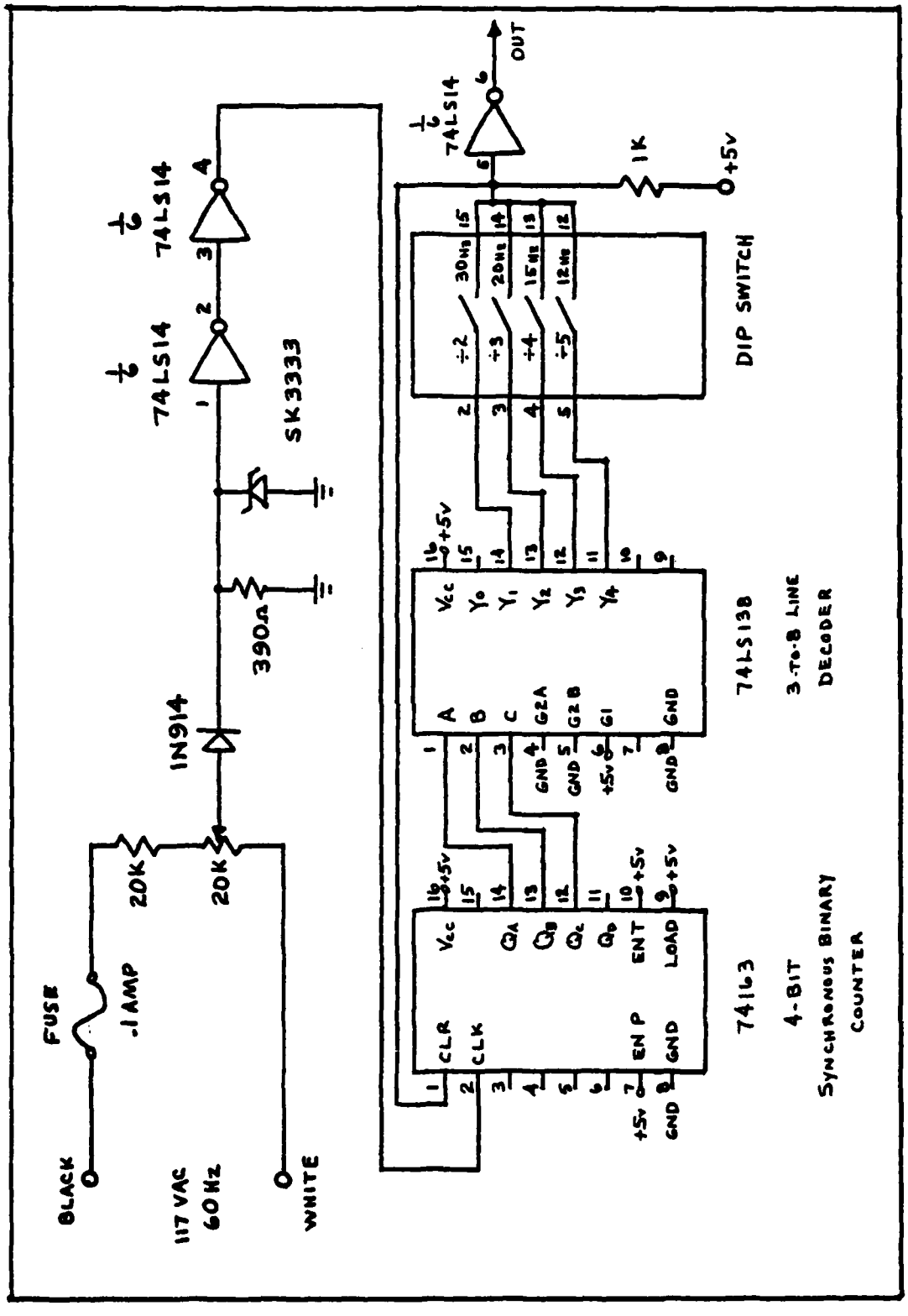

Figure III-9. Vertical Synch Pulse Generator

clear input of the counter and also inverted to become the usable output signal. Any one of the DIP switches may be selected for the desired output frequency. This circuit, therefore, produces a 30 Hz, 20 Hz, 15 Hz, or 12 Hz output.

Testing

The circuit was tested after being constructed by first connecting the output to an oscilloscope and frequency counter. Sixty Hz was correctly divided into the proper TTL pulses at the selected output frequencies. This signal then replaced the Wavetek signal generator that was connected to the scan-start pulse generator. Set at 30 Hz, the vertical synch pulse generator kept the Reticon video sample output synchronized without an error-producing beat frequency pulse being present.

Different amplitudes of video sample output can be selected by choosing one of the selectable VSPG frequencies. A lower frequency selection, such as 12 or 15 Hz, causes a longer integration delay time that produces a larger voltage sum from each of the photodiodes. It was decided that frequencies less than 30 Hz or 20 Hz could possibly allow "dark current" values to produce errors in brightness and contrast calculations. The 30 Hz rate was finally determined to be the best overall frequency for the VSPG after studying the Reticon scan and data table values.

USER-INTERFACE CONTROL CONSOLE

The functional design for the user-interface control

console was kept the same as Baxley described in his thesis. An experimenter box (5 1/16 x 2 5/8 x 1 5/8 inches), consisting of a plastic body and aluminum cover, was purchased to house the master reset switch, switches 1 through 4 (S1-S4), and the brightness and contrast light-emitting diode (LED) displays.

The aluminum cover was replaced by dark red Plexiglas so that the LED displays could be seen without mounting them on the exterior. Switches S1-S4 and the master reset switch were mounted on the Plexiglas for easy access in operating the controller (see Figure III-10).

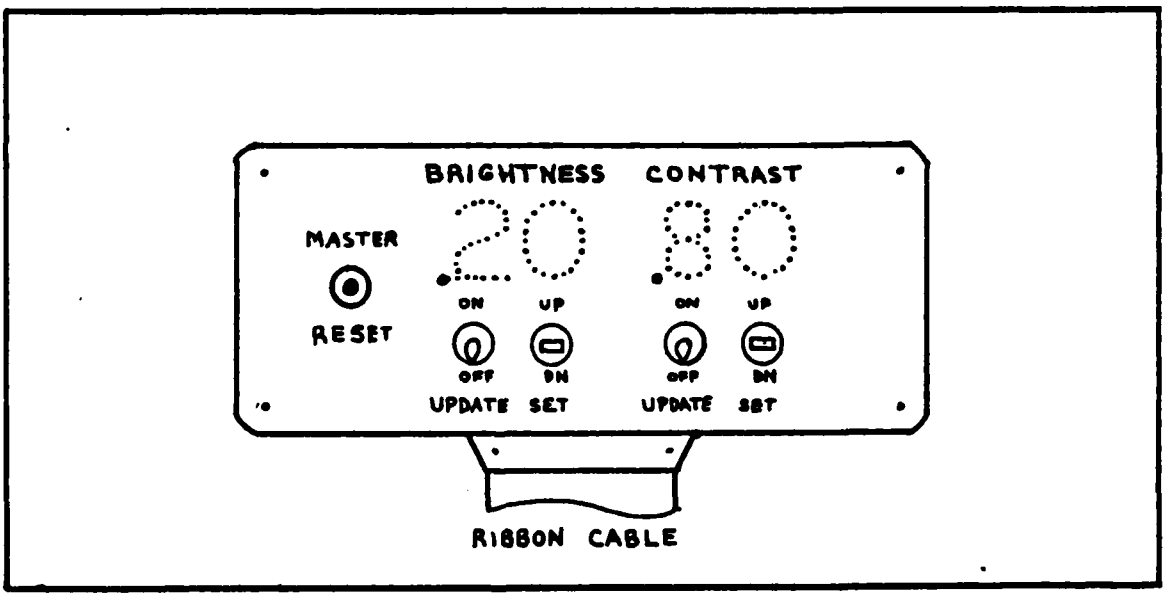

Figure III-10. User-Interface Control Console

Brightness and contrast values are input to the controller by the set switches, S1 and S2, respectively. Both of these switches are momentary double-pole single-throw (DPST), three-position switches, with the center

position off (on-off-on). The update switches, S3 and S4, are single-pole single-throw (SPST), two-position switches which are used to signal that the brightness and/or contrast values which are presently in the computer are to be updated. The master reset switch is a momentary single-pole single-throw (SPST) push button which applies ground when pressed to the MDX-CPU2 computer board for a power-on reset.

Numerical values for brightness and contrast are displayed by the TIL-311, single digit LEDs. Two LEDs, representing values from 00 to 39, are used for brightness, and two LEDs, representing values from 00 to 99, are used for contrast. The left decimal points of LED D1 and D3 are used to tell the user the status of the data entered. When the decimal point is lit, the value displayed has not yet been entered in the computer by the update switches.

A 26-conductor ribbon cable connects the control console to the rest of the controller circuitry. The console may be disconnected from the rest of the controller and/or ribbon cable by the 26-pin header connector mounted on the console.

The control console was tested as an integral part of the total controller system and not as an independent syb-system. A description of how the control console is used in conjunction with the rest of the controller is presented in Chapter V.

POWER SUPPLY/VOLTAGE REGULATOR

The incomplete controller hardware was being powered by

several independent power supplies. A Power-One, Inc., Model HCBB-75W, from the AFIT lab had been mounted inside the controller cabinet to provide +5 vdc, +12 vdc, and -12 vdc to part of the hardware. Other laboratory external power supplies were being used to supply +5 vdc, + and - 12 vdc, and + and - 15 vdc to different portions of the controller hardware. In an effort to begin packaging the controller, current measurements were made of each separate supply in order to determine the total system power requirement.

The existing internal power supply was adjusted from + and - 12 vdc to + and - 15 vdc. A voltage regulator circuit which added the availability of 12 volts was then designed and added to the internal supply in the controller cabinet. A 7812CT fixed voltage regulator (+ 12 vdc) and a 7912CT fixed voltage regulator (- 12 vdc) were used along with input and output filter capacitors (see Figure III-11).

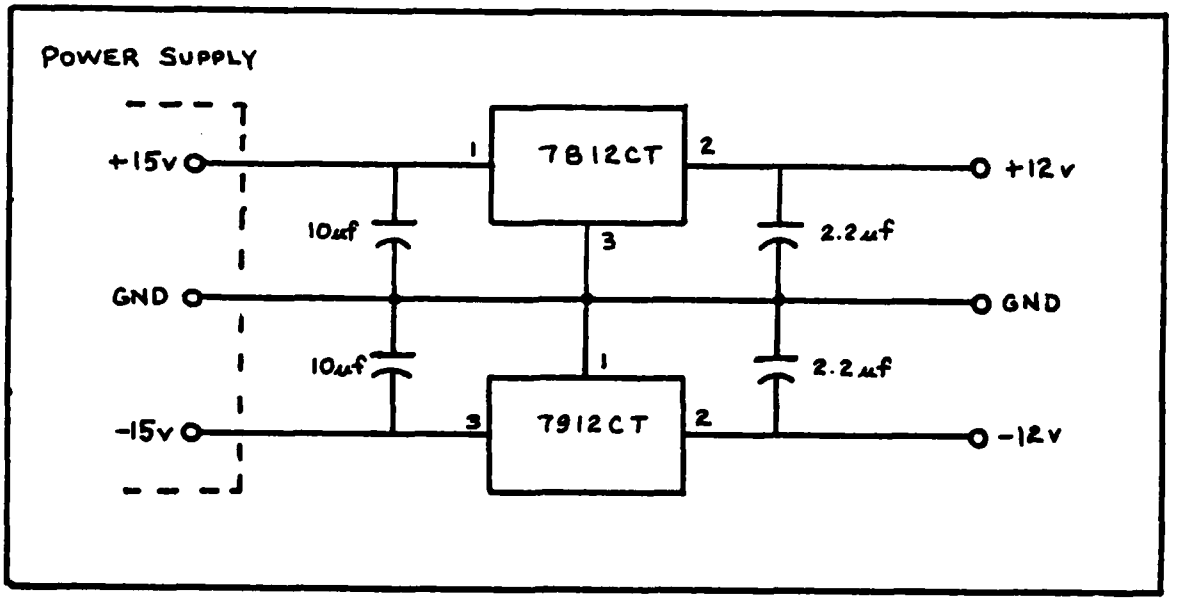

Figure III-11. 12 Volt Regulator Circuitry

After testing the controller while using the all-in-one supply, a short power discontinuity began to develop, first at random, then at an even interval of 21 seconds. This discontinuity only began after the controller had been operating for about eight to ten minutes, and would appear as a momentary power loss. It was most evident in the 5-volt supply, but could also be seen on the 12- and 15-volt lines.

Since it seemed that the 5-volt portion of the supply was failing, a power supply with a larger current capacity for the 5-volt section was chosen. A Sierracin/Power Systems, Model 5CX515TA, power supply with a 5-volt, 10-Ampere rating was used. This solid-state, +5 and + and - 15 volt supply eliminated the power discontinuity. No further problems due to power supply inadequacy have occurred.

SUMMARY

This chapter described the design, construction, and testing of the controller sub-systems which were undertaken in this thesis. The next chapter will describe the software which operates the controller.

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IV CONTROLLER SOFTWARE

After the hardware, which was described in Chapter III, was designed and built, it had to be tested both independently as a sub-system and, most importantly, as a total controller system operated by the controller software. This chapter first describes each subroutine which Baxley developed in his thesis (Ref 5:77-87) and was first used in testing the controller in this thesis. The modifications to this software are then described at the end of this chapter.

SOFTWARE ROUTINES

Initialization (INIT)

INIT initializes the controller when the controller is first turned on or when the master reset switch is pressed. It first clears all random access memory (RAM) in the MDX-CPU2 and then initializes the external hardware by toggling the output status bits, except bit 3. This clears any arbitrarily set flags which might have been set while power was turned on and initializes the desired brightness and contrast counters to the values preset by switches S5 and S6. As a last step, INIT calls the brightness update (BUPDAT) and contrast update (CUPDAT) routines which loads the desired brightness and contrast values into the CPU.

Clear Memory (CLRMEM)

CLRMEM is called by INIT to clear a block of memory for the scratch pad work area and Reticon data table. The

starting address of the block is specified by the HL register pair and size of the block is defined by BC.

Executive (EXEC)

EXEC is the main program in the software. It endlessly repeats itself, calling the other routines in the proper order: SCAN -- read Reticon scan; AVGBRT -- compute average brightness; CNTRST -- compute overall contrast; BADJ -- compute brightness; CADJ -- compute contrast; and EXEC -- call itself for an endless loop.

Status Update (STEST)

This routine checks the input status port (ISPORT) to see if the user wishes to update desired brightness or contrast. The brightness update bit (bit 0) is first checked, and BUPDAT is called if the bit is set. The contrast update bit (bit 1) is then checked, and CUPDAT is called if this bit is set. The routine returns to EXEC when complete.

Brightness Update (BUPDAT)

BUPDAT updates the stored desired brightness value, DBRT. The unscaled desired brightness value, UDBRT, is read from the input brightness port (IBPORT) and saved. This value is then converted to a scaled, binary balue and saved. Bit 0 of the output status port (OSPORT) if finally toggled to signal the hardware that the desired brightness has been

updated.

Contrast Update (CUPDAT)

CUPDAT updates the stored desired contrast value, DCON. It first reads the unscaled desired contrast value, UDCON, from the input contrast port (ICPORT) and saves it. The value is then converted to a scaled binary value and saved. Bit 1 of the output status port (OSPORT) is toggled to signal the hardware that the desired contrast has been updated.

Decimal to Binary Conversion (CONVRT)

This routine converts an eight-bit binary-coded decimal (BCD) number located in the A register to its binary equivalent. The result is left in the A register.

Divide (DIVIDE)

The DIVIDE routine divides a 16-bit unsigned integer in register pair HL by an eight-bit unsigned integer in the C register. The eight-bit answer is left in the L register with the least significant bit (LSB) rounded up if the remainder is greater than 0.5. The remainder that existed before rounding is in the H register.

Scan (SCAN)

The SCAN routine reads 512 bytes of data from the input data port, IDPORT. Data are read by using the block input with increment command, INIR, for a minimum read time with

no waiting for handshakes. External hardware is synchronized with the Z80 by the reset pulse which SCAN sends to the wait-state controller.

Brightness Calculation Routine (AVGBRT)

This routine computes the average brightness of the 512 samples measured by the Reticon array. AVGBRT first calls the table summing routine, SUMTBL, to calculate the total sum of the 512 samples. The average brightness is then calculated by dividing the table sum (TSUM) by 512. The eight-bit result is rounded up one bit if the remainder is equal to or greater than 0.5, and then stored as ABRT, average brightness.

Table Summing (SUMTABL)

SUMTBL sums the 512 sample values that are stored in the 512 sample block, TABLE. The routine initializes the DE register pair at the first byte of the first page, then calls ADPAGE to add all the bytes on that page. The sum of the first page is loaded in the BC register pair, and then added to the value in the HL register pair when the second page is summed. The end result is saved in three bytes in TSUM with an overflow (carry bit) in TSUM's most significant bit (MSB).

Page Addition (ADPAGE)

This routine sums the memory page (256 bytes) by using

a loop with the beginning of the page addressed by the DE register pair. The page sum is located in the HL register pair at the end of the routine for use by the calling routine, SUMTBL.

Actual Contrast (CNTRST)

CNTRST is the routine which computes the actual contrast of the sine-wave grating on the video monitor, the find maximum value (FMAX) routine and find minimum value (FMIN) routine are called to find the maximum and minimum sample values (BMAX and BMIN) in the data table. Average brightness (ABRT computed by AVGBRT routine), BMAX and BMIN are used to compute actual contrast (ACON) in the formula (3) below:

$$ACON = \frac{256 \times (BMAX - BMIN)}{(2 \times ABRT)} \qquad (3)$$

ACON is scaled by pre-multiplying the true contrast by 256 so that integer, rather than fractional, values need only be computed.

Find Max (FMAX)

This routine is used to find the maximum sample value stored in the Reticon data table. FMAX begins searching with the third sample since the first two samples are inconsistent with the rest of the table (Ref 5:43).

Find Min (FMIN)

FMIN is similar to FMAX except that it searches for the minimum value in the data table rather than the maximum. The first two data samples are also ignored by this routine.

Brightness Adjust Routine (BADJ)

BADJ compares the value for actual or average brightness (ABRT) with the value for desired brightness (DBRT). If these two values differ, a brightness correction value is sent to the brightness output port, OBPORT. The old value for brightness out, BRTOUT, is either incremented or decremented one bit at a time until the new brightness value is equal to the desired brightness.

Contrast Adjust Routine (CADJ)

Values for desired and actual contrast (DCON and ACON) are compared in this routine. If the two values differ, a contrast correction value is sent to the contrast output port, OCPORT. Contrast is either incremented or decremented one bit at a time until the new value for contrast is equal to the desired contrast value.

MODIFICATIONS

The majority of this thesis effort involved using controller software which Baxley had designed in his thesis. After closing the brightness control and contrast control loop for the first time, the controller software could then be extensively tested. As with any software, the minute

problems associated with it are not known until it is tested under realistic conditions.

After analyzing the Reticon scan video out signal from the sampling circuit on an oscilloscope, it was seen that it might prove beneficial to modify the software. First of all, with the video monitor adjusted to a particular brightness out, the Reticon scan showed a larger brightness output at the center of the CTR. Brightness tapered off slightly, but noticably, from the center to the top, the bottom, or either side. A Spectra Pritchard Photometer verified that the Reticon was actually correct in seeing this brighter output in the center of the screen. Martindale found similar data when he sampled the center vertical portion of a video monitor (Ref 3:33-35).

Secondly, the Reticon's scan showed a slow rise time at the beginning and a slow fall time of several sample widths at the end of the 512-sample data block. Baxley noted this characteristic of the fist two samples (Ref 5:43) and therefore designed the software to ignore the first two samples in the calculations. The Reticon product brochure (Ref 6:4) neglects the first two, and the last two, photodiode values in its specifications.

A third characteristic noted of the Reticon scan was the inaccurate and nonuniform sample values from photodiodes #350 to #354. The error of these samples is proportional to the magnitude of the brightness sampled. Baxley also noted this nonuniformity but believed that the error from these

samples would not affect the computed average brightness (Ref 5:44). Placement of the ribbon cable did not seem to change the magnitude of error in these five photodiodes.

With these three characteristics in mind, it was decided that a more accurate software program could be developed for the controller. A decision to use only the photodiode sample values in the middle of the 512-sample data block was made. By using the middle portion (128 samples) of the Reticon scan (192 + 128 + 192 = 512), calculation errors due to the nonlinearity of the CRT, beginning and ending samples read error, and inaccuracy of photodiodes #350 to #354 could be eliminated.

In order to modify Baxley's software to compensate for the recommendation mentioned above, four routines (AVBRT, SUMTBL, FMAX, and FMIN) were changed and one routine (ADPAGE) was deleted.

Brightness Calculation (AVGBRT)

This routine computes the average brightness measured by the Reticon array. Some 128 of the 512 samples are used for the brightness calculation and represent the center portion of the Reticon scan (192 + 128 + 192 = 512).

AVGBRT calls the summing routine (SUMVAL), which sums the center 128 photodiode samples. This sum is then rounded to eight most significant bits and divided by 128. The result is rounded by checking to see if bit 7 is set. If it is not set, the value is left alone, and if it is set, the value is rounded up. This value is now the average

brightness value for the middle 128 samples and is saved as ABRT in location F802H.

Summing Routine (SUMVAL)

SUMVAL sums the 128 samples of interest of the middle portion of the data table. This 128-sample portion begins at address F9C0H of the data table (TABLE) and continues through FA3FH.

The DE register pair is set at the beginning of the start value and the counter, BC register pair, is set for 128 counts. Each of the 128 values is read and added to the previous sum until all are summed. The final result is saved as SUM (two bytes) in locations F832H and F833H.

Find Maximum Value (FMAX)

This routine is similar to Baxley's FMAX except that it is made to find the maximum value in the interest area of 128 values. As each value is pointed to, it is compared to the previous value to determine which value is larger. When the loop is finished, the maximum brightness value (BMAX) is saved in location F830H.

Find Minimum Value (FMIN)

The FMIN routine is identical to the FMAX routine except that it searches for the minimum value in the 128-byte area of interest rather than the maximum value.

SUMMARY

The Assembly language source listing for the modified controller software is included as Appendix D. The last phase of this thesis involved working with this new program to more accurately operate the controller.

V SYSTEM OPERATION

This chapter contains a description of the controller as it should be packaged once all the circuitry is wire-wrapped, and how to operate it for controlling brightness and contrast.

CONTROLLER ENCLOSURE

The finished prototype controller should be contained in three separate enclosures: main chassis, Reticon circuitry and lens assembly, and user-interface console. The Reticon circuitry and lens assembly sub-assembly is connected to the main chassis by a shielded, multi-conductor cable which will allow the larger main chassis to be placed in a convenient location out of the way. The user-interface console is connected to the main chassis by a 26-conductor ribbon cable approximately six to eight feet in length, allowing the controller operator to move around while operating the system, but remaining out of the way. Figure V-1 depicts the controller packaging concept in a typical testing arrangement.

The main chassis, which already contains the power supply/voltage regulator circuitry and Mostek MPX-CPU2 boards, will contain the wire-wrapped circuit boards of circuitry other than the Reticon motherboard and array board. The on-off switch mounted on the main chassis is the only power switch to the complete controller and will power up the system to the preset initial values for brightness

and contrast when activated.

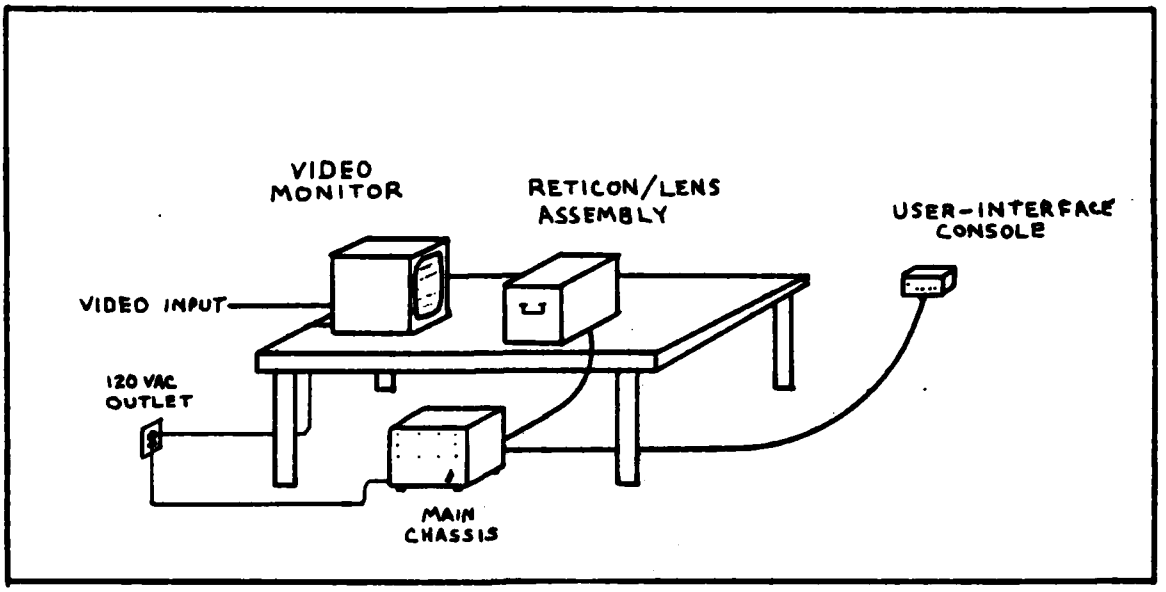


Figure V-1. Packaged Controller Concept

The Reticon circuitry and lens assembly enclosure houses both the Reticon motherboard and photodiode-array board, along with the lens assembly. The lens assembly consists of the lens and the three-axis adjustable mounting assembly on which the array board is mounted. This portable enclosure can be easily moved into a position and adjusted so that the sine-wave grating from the video monitor is focused onto the photodiode array. When not using the controller during vision testing, this enclosure may be moved out of the way.

The user-interface console is the hand-held control box which the operator uses to communicate with the controller. Since this is a separate unit with a long ribbon cable, the operator does not have to stand close to the monitor to

operate the controller.

OPERATION

In normal operation, the operator turns the system on by the power on-off switch located on the master chassis. When the system is initialized, the preset values for brightness and contrast (set by S5 and S6) are displayed on the user-interface console automatically. The operator then has the option of changing the values to new desired values, and also updating the desired values stored in the computer.

Two pairs of LED displays are used to show the desired brightness and desired contrast values. Switches located below the displays control data entry, and a master reset switch resets the controller to the preset values.

Brightness is variable over the range of 0 to 39 fL in single unit increments by the brightness set switch. If, for example, brightness is to be increased from the present setting, the brightness set switch is held up (or down) until the new desired value is reached. A dual-rate clock increments (or decrements) the setting at about one unit per second for the first four counts, then automatically switches to about a four-unit-per-second count rate until the set switch is released. By using this dual-rate clock feature, the operator can quickly set the brightness to any desired value between 0 and 39 fL. If a desired value has been overshot, the set switch can be toggled in the other direction back to the correct value.

Contrast is variable over the range of 0 to 99 percent

in single unit increments by the contrast set switch. The desired value of contrast is obtained in the same manner as in the brightness example described above. The same dual-rate clock circuit is used for both brightness and contrast.

The desired brightness and/or contrast values are sent to the controller computer by update switches located beside the set switches on the user-interface console. The console has separate update switches for brightness and for contrast. There are two modes in which the operator can update the desired brightness and contrast values stored in the computer. When an update switch is in the on position, the desired value is immediately sent to the computer by the input port as the displayed settings are changed. When an update switch is in the off position, the desired value is not sent to the computer. This feature allows the operator to set up a new value for desired brightness and/or contrast while the controller's brightness and/or contrast control circuits remain fixed at the prior setting. Whenever the operator decides to update the signal to the control circuits, he can then toggle the update switch on, then off.

Both brightness and contrast displays on the user-interface console have an LED flag denoted if the desired value has been updated or not. The left-most decimal point on both displays is used for this flag function. If the brightness setting is changed while the brightness update switch is off, the brightness LED flag will light, indicating that actual brightness is still set at the

previous setting. If the update switch is toggled on and off, the LED flag will go off and the brightness control circuit will change its setting to the new value. When the update switch is left in the on position while the desired brightness value is continuously changed, the LED flag will blink on and off, indicating that the value is being updated about every 40 milliseconds (Ref 5:32). The light will go off as soon as the set switch is released, denoting the currently displayed desired brightness value has been received by the computer and is being sent to the brightness control circuitry.

The update switch for contrast works identically to the brightness update switch. The contrast display also uses the left-most decimal point of its display for the LED flag indicator light.

SUMMARY

This chapter described the three enclosures which make up the controller system and their typical layout for vision testing. The operation of the user-interface console for changing and updating desired brightness and contrast values was also explained.

VI CONCLUSIONS AND RECOMMENDATIONS

CONCLUSIONS

The breadboarded hardware circuitry which was developed in Baxley's thesis was used during this thesis in an effort to finalize a working-model prototype controller. As stated in Chapter I, this thesis was based on the assumption that Baxley's evaluation and redesign of the controller were correct and did not require any in-depth re-evaluation.

It had also been assumed that Baxley's hardware circuitry would be provided in the form of wire-wrapped boards in ample time so that the complete packaging of the controller would be accomplished. Since these boards were not available, it was necessary to trouble-shoot the breadboard construction on several occasions due to the breadboard contact tension diminishing. Although a greater knowledge of the existing circuitry was obtained through trouble-shooting, valuable time, which could have been spent testing the software, was lost.

The circuits which were designed and constructed in this thesis were tested as individual sub-systems and as integral parts of the total controller system. The user-interface console was designed, built, and tested as an important step in the process of packaging the prototype controller. In order to close the double-feedback control loop, the brightness and contrast control circuits, along with the vertical synch pulse generator, were designed, constructed and tested so that system performance and

software routines could be tested as a total system instead of just independently. Controller software was modified so that a more accurate representation of the video monitor's sine-wave grating might be sampled, digitized, and controlled by the total system.

The last step in packaging the controller, which includes wire-wrapping the circuits, remains to be done, along with final calibrations with the sine-wave grating generator.

RECOMMENDATIONS

With the assumption that the beginning concept and design of the controller is to be used, only the final packaging and testing of the controller with the modified software is left to be done. Once this is completed, a working controller prototype will be available to assist in AFAMRL's vision testing research.

Since the beginning of the controller's first concept, AFAMRL has begun using an Optronix, Series 200, Vision Tester which contains a Rockwell AIM-65 computer test system with an Optronix video generator circuit board. This 6502-based microprocessor system automatically selects a contrast value based on preset internal data for the Optronix generator to produce, while the brightness of the video monitor is kept at a fixed value. The person taking the contrast sensitivity test presses a button when a sine-wave grating pattern becomes just visible on the monitor's CRT.

The system also automatically randomizes the increasing contrast slew rate and changes the spatial frequency of the grating so that more accurate test results can be obtained.

With the advent of this new testing process being used at AFAMRL, the controller developed in this thesis must be modified so that it may be used in conjunction with the Optronix/Rockwell system. By doing this, it may then be used as originally intended in calibrating the video generator test system, or in keeping the brightness and contrast immune from line voltage fluctuations and calibration drift during the test session.

A modification to interface the controller with the Optronix/Rockwell system could be made by tapping the brightness 8-bit control word and the contrast 12-bit control word which signals the video generator of the new desired value. These data lines would be connected to the controller's input port 0 (brightness) and input port 1 (contrast), enabling the values to be both displayed on the user-interface console and routed to the Mostek MDX-CPU2 controller computer (see Ref 5:52 or Appendix A). Since the video generator uses 12 bits for contrast control, the thesis controller would be connected to the eight most significant bits of the generator. The controller software would then be modified so that a scale factor and time-sampling modifications may compensate for the 12-to-8-bit conversion. The outputs of the desired brightness and contrast counters (U11 and U14) would be disconnected by a relay activated switch so that the test operator could

choose which source the desired values were input from -- the user-interface console of the controller or the Optronix/Rockwell system.

An advantage of connecting the two systems would be the capability for the controller to track the variable slew rates which the Optronix/Rockwell system produces, rather than a test operator manually toggling the controller's set switches for changing the brightness/contrast. The Optronix/Rockwell system also has the capability for recording the value at which the person taking the test sees the grating and signals the system. It can store these values and compute a person's contrast sensitivity rather than the test operator having to manually record data and perform calculations.

To directly connect to the thesis controller, the 8- and 12-bit Optronix/Rockwell control word would have to be either in BCD (binary coded decimal) form as required at this circuitry point in the thesis controller, or input to a binary-to-BCD decoder circuit. The desired brightness and desired contrast inputs would each require this type of decoder circuit if the Optronix/Rockwell system outputs a binary control word to the Optronix. If the Optronix/Rockwell has a BCD output control word, the decoder will not be necessary.

Upon final completion of the packaging and modifications to make the thesis controller fully useful, calibration adjustments must be made to finally set the

calibration standards for which this system was intended.

APPENDIX A

BAXLEY'S HARDWARE CIRCUITRY SCHEMATICS

This appendix contains the controller circuitry schematic diagrams and timing diagrams for the electronic circuitry which Capt. Baxley had constructed in his thesis project. They are included here so that all necessary data will be contained in this thesis, making it a complete and informative document for the controller (Ref 5:50-76).

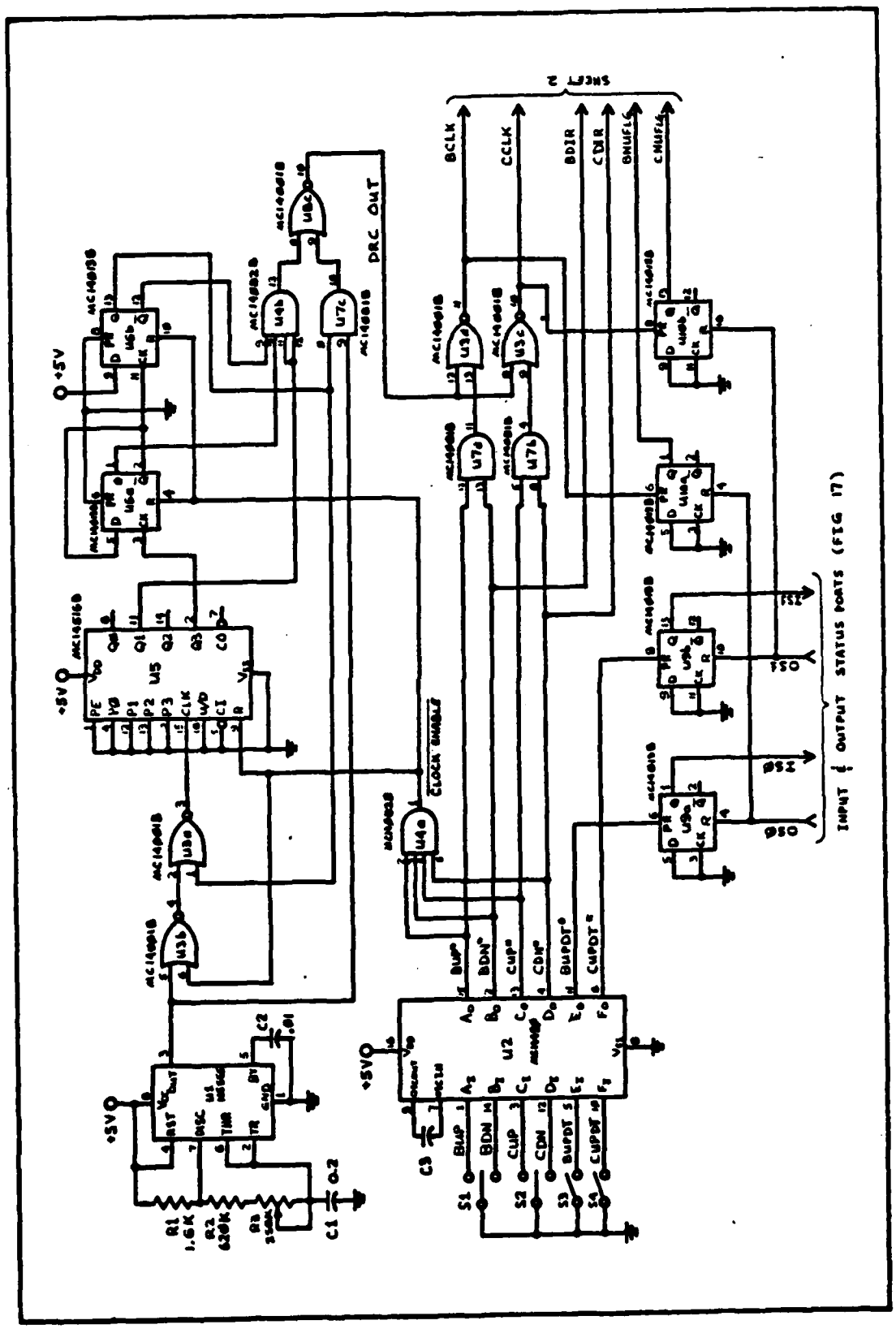


Fig 8. (Sheet 1) User-Interface Circuits Schematic

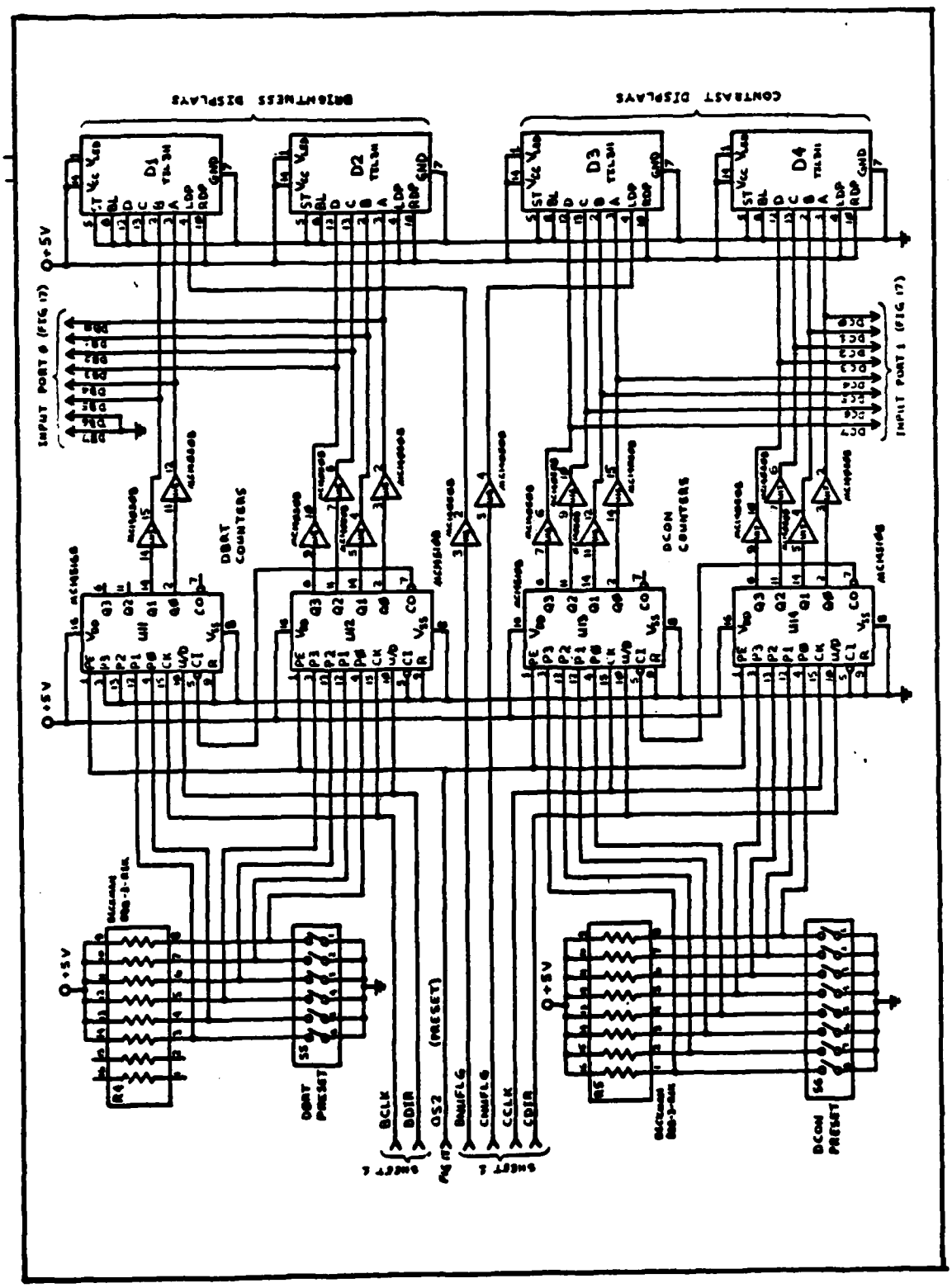


Fig 8. (Sheet 2) User-Interface Circuits Schematic

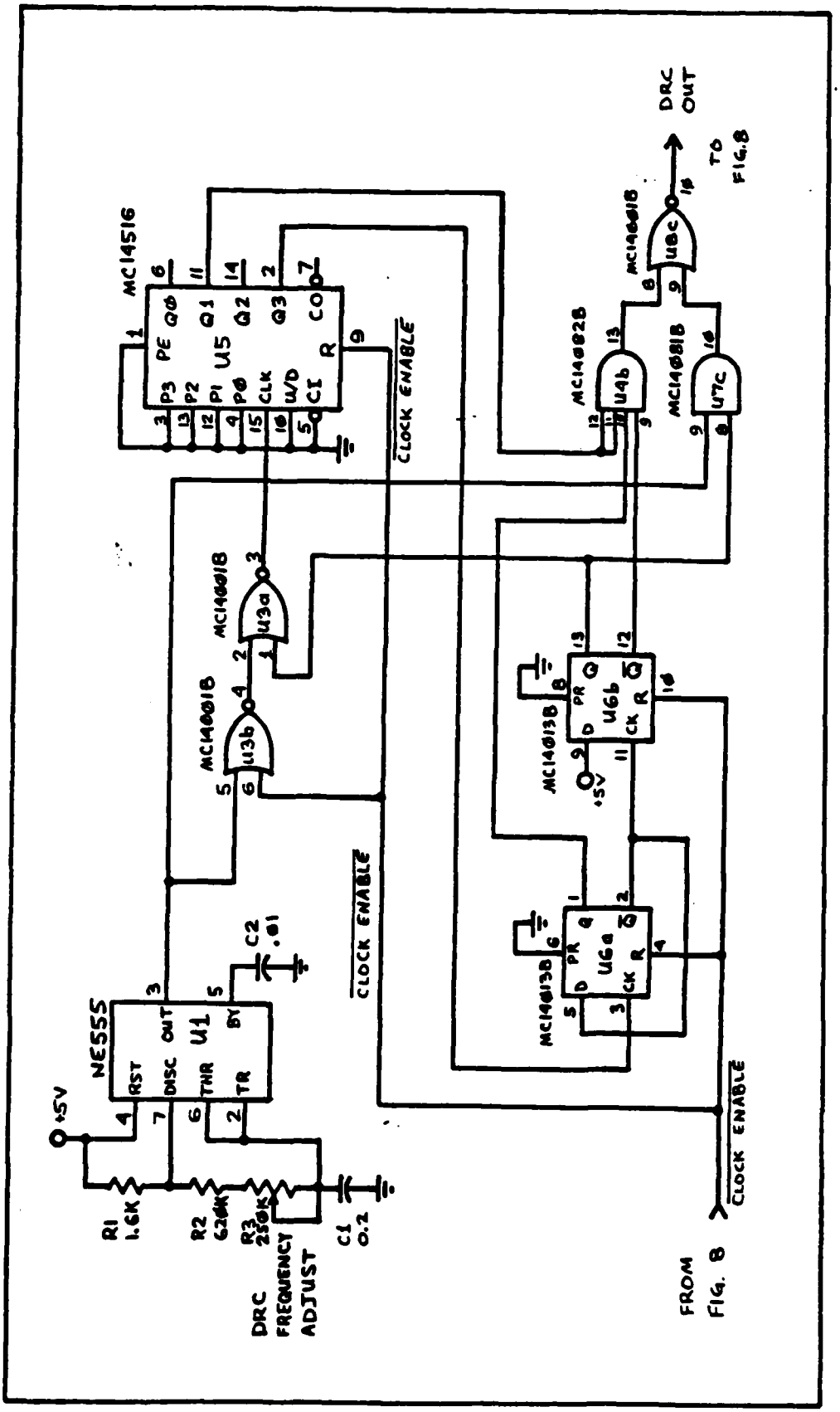


Fig 9. Dual-Rate Clock (DRC) Schematic

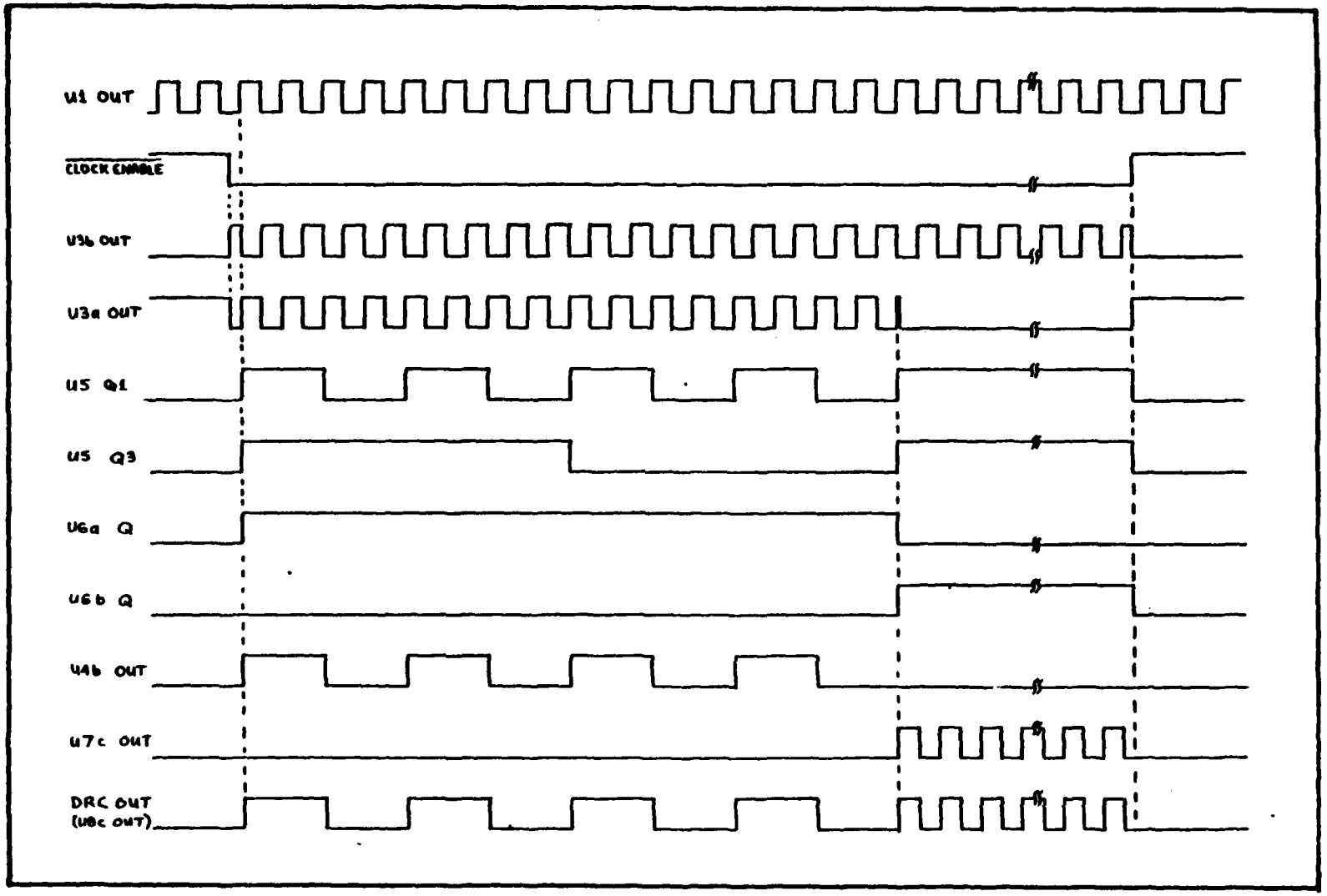


Fig 10. Dual-Rate Clock (DRC) Timing Diagram

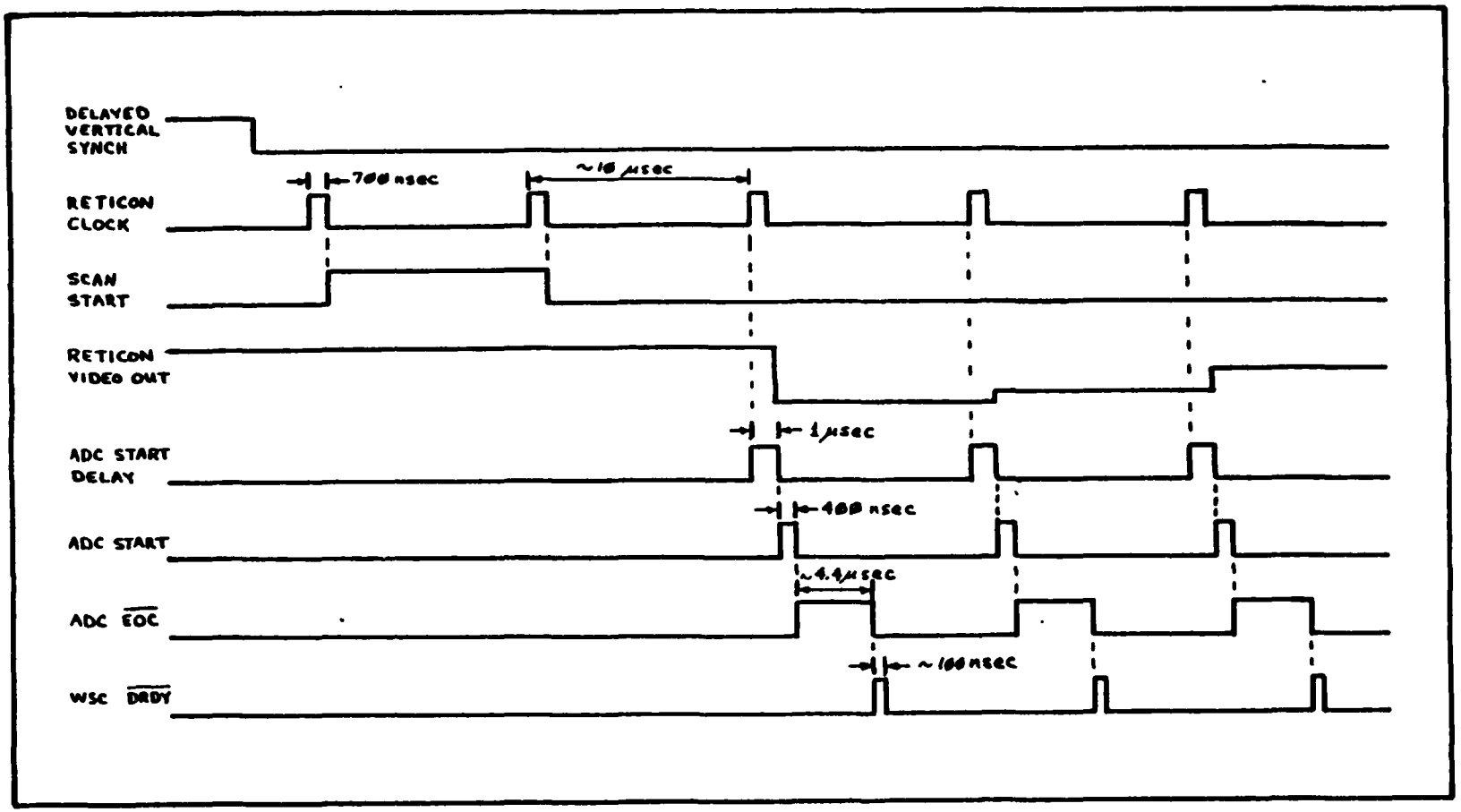


Fig 11. Reticon Circuits Timing Diagram

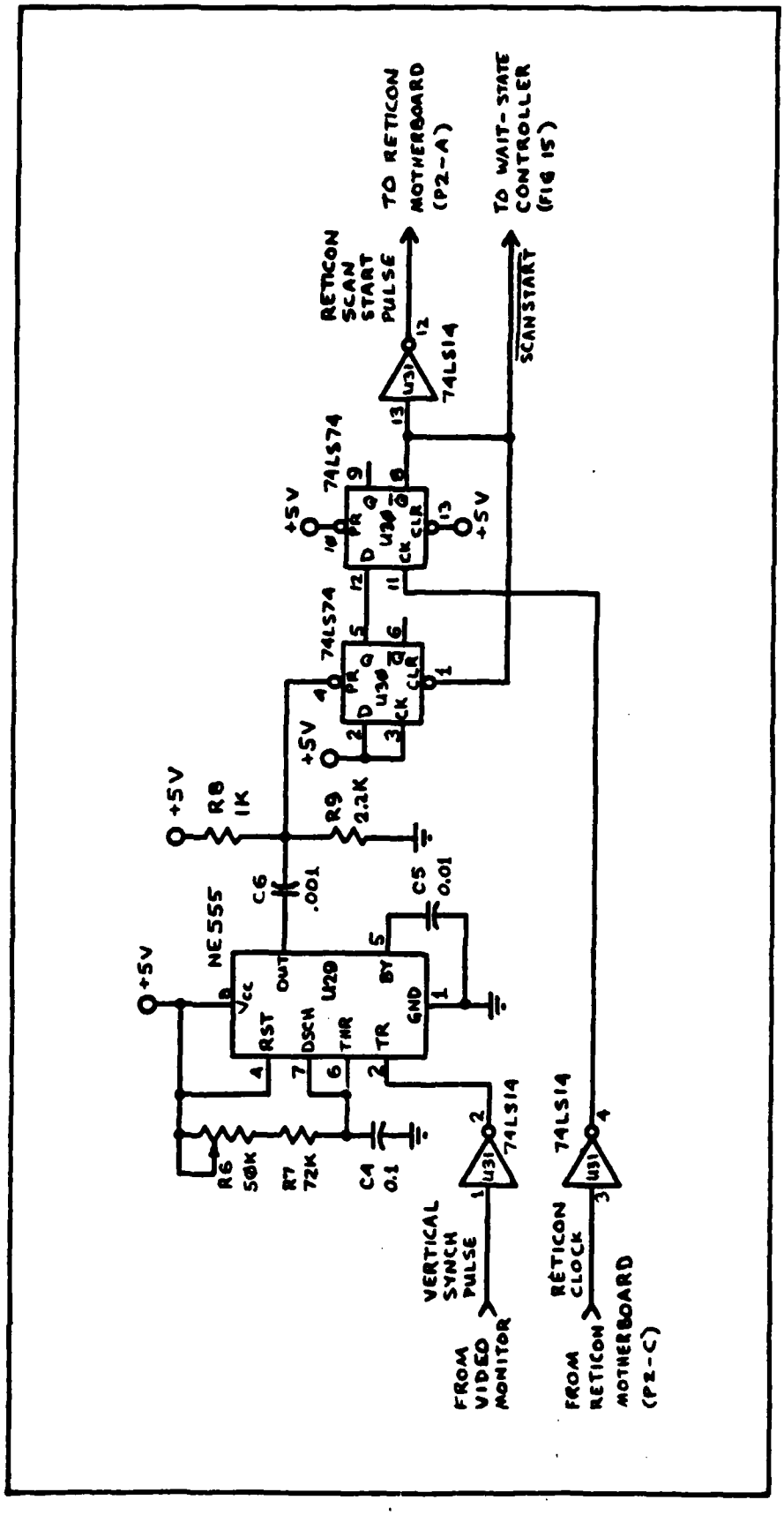


Fig 12. Scan-Start Pulse Generator (SSPG)

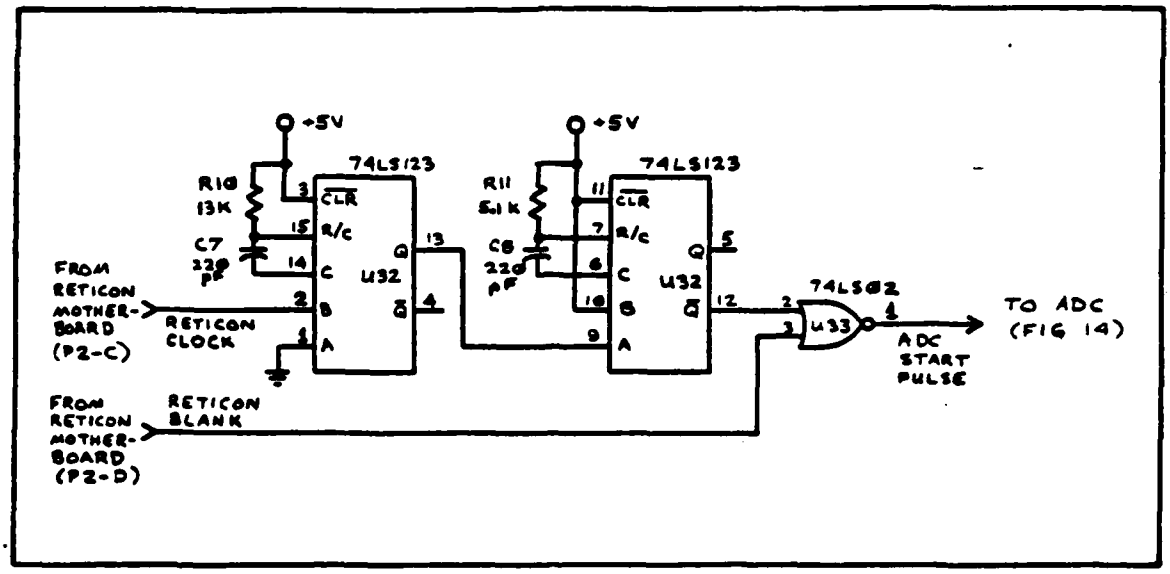


Figure 13. ADC Start Pulse Generator

Figure 13, is controlled by the Reticon's Blanking Pulse, which is low during scans, and high otherwise. Thus, ADC Start Pulses are generated only during scans of the monitor.

Inverting Amplifier and Analog-to-Digital Converter

These circuits are shown in Figure 14. The Inverting Amplifier is simply a 741 op-amp configured as an inverter. R14 sets the gain of the inverting amplifier. R15 was selected to minimize the input bias current error (Ref 10:AN20-1).

U35 is a Datel ADC-HZ12BGC analog-to-digital converter, set for 8-bit short-cycled operation. This circuit was set up as outlined in Datel's Product Handbook (Ref 11:44-47).

U35 begins a conversion when triggered by the ADC Start Pulse Generator. The End-of-Conversion (EOC') output goes

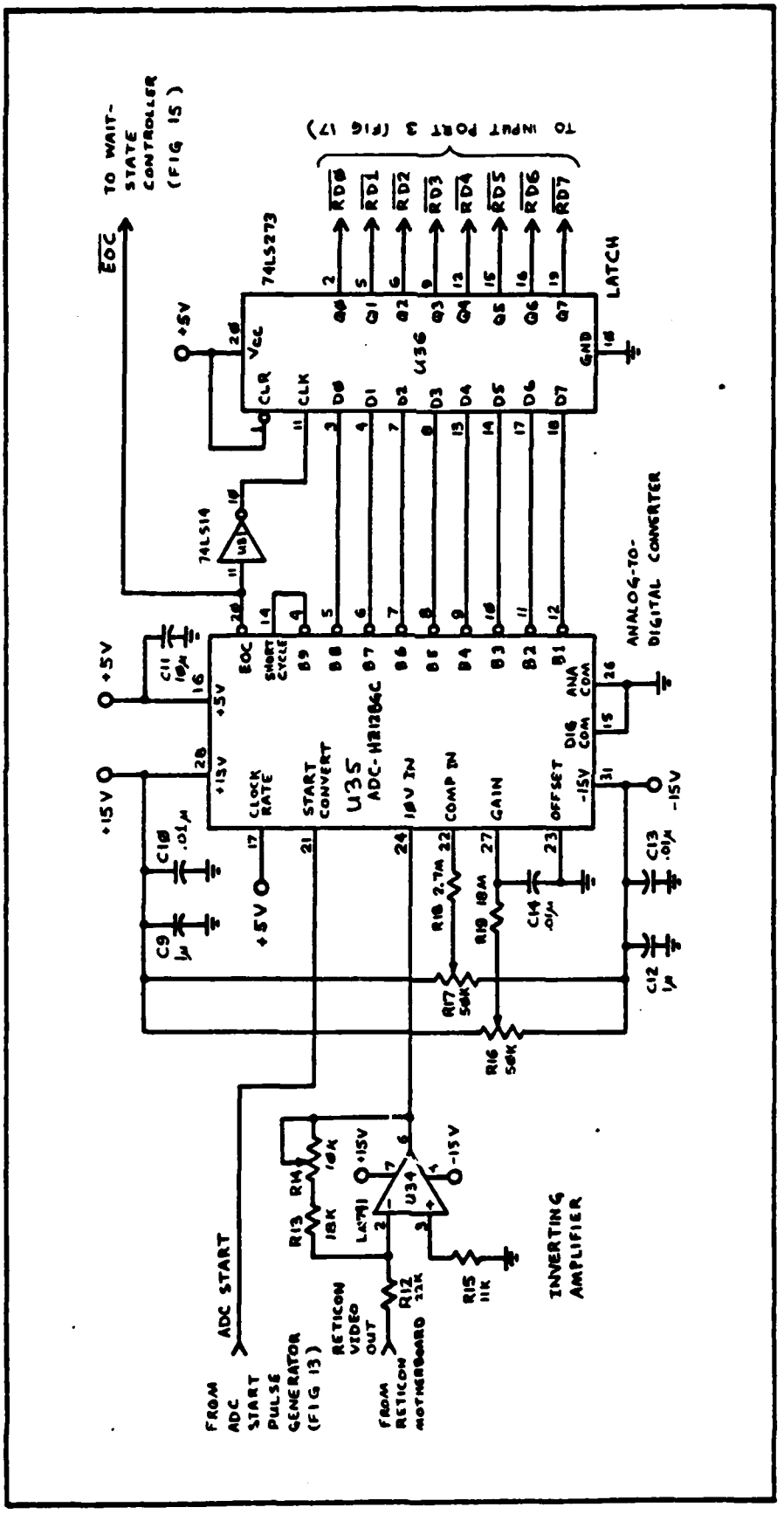


Fig 14. Inverting Amplifier and A/D Converter

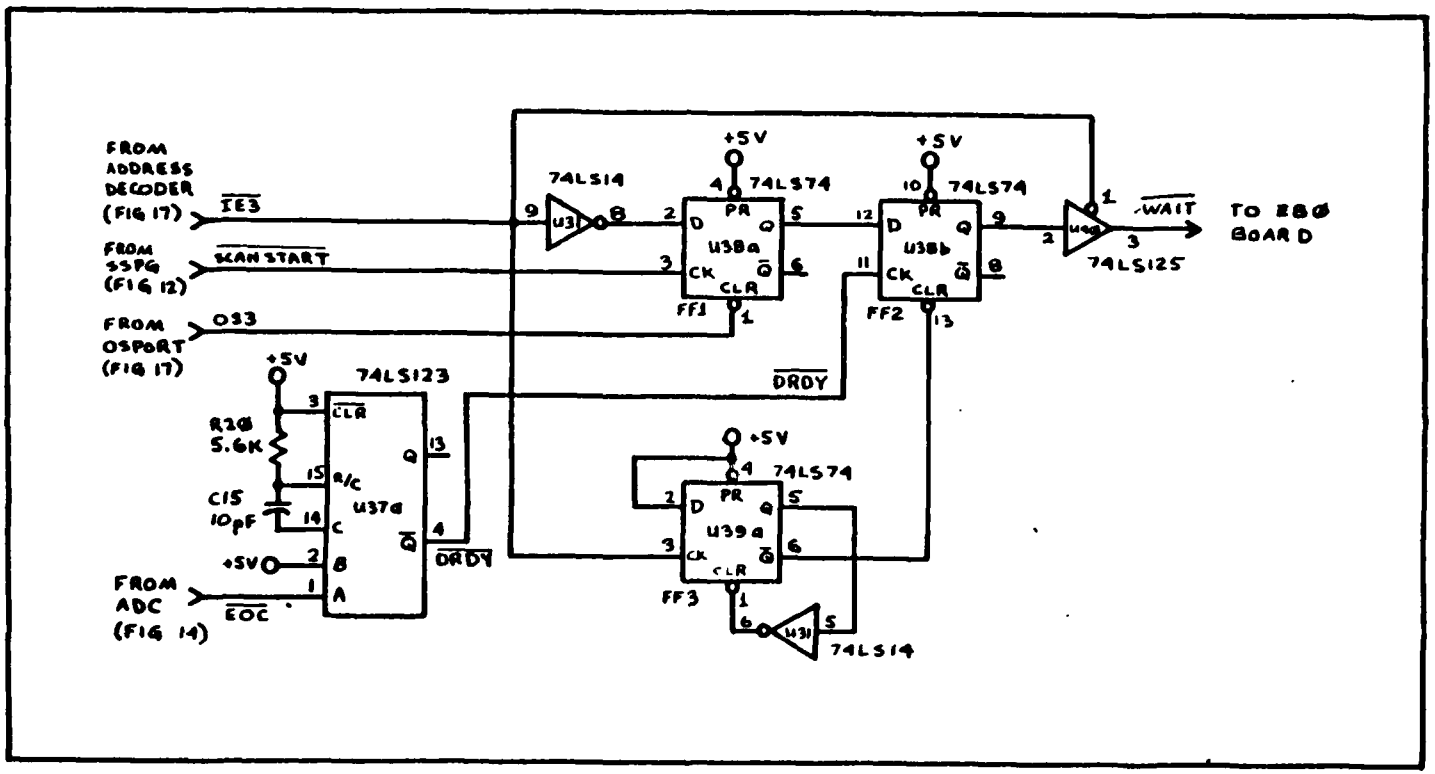
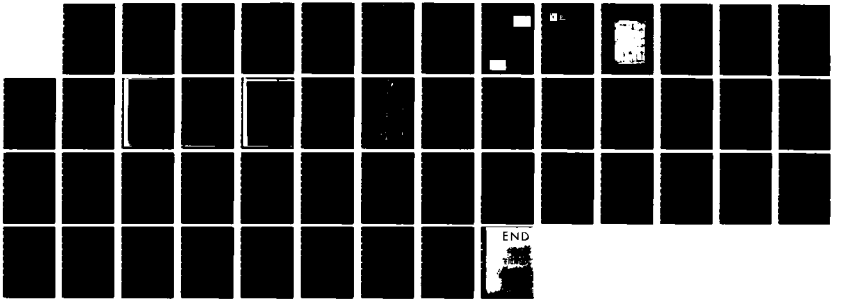
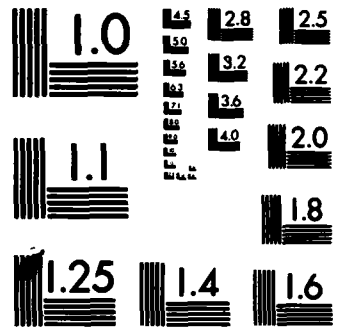


Fig 15. WAIT-State Controller (WSC) Schematic

AD-A138 294 AN AUTOMATIC SINE-WAVE GRATING CONTROLLER TO BE USED FOR CONTRAST SENSITI.. (U) AIR FORCE INST OF TECH WRIGHT-PATTERSON AFB OH SCHOOL OF ENGI.. M H SWANN 2/2

UNCLASSIFIED 05 DEC 83 AFIT/GE/EE/83D-65 F/G 9/1 NL





MICROCOPY RESOLUTION TEST CHART
NATIONAL BUREAU OF STANDARDS-1963-A

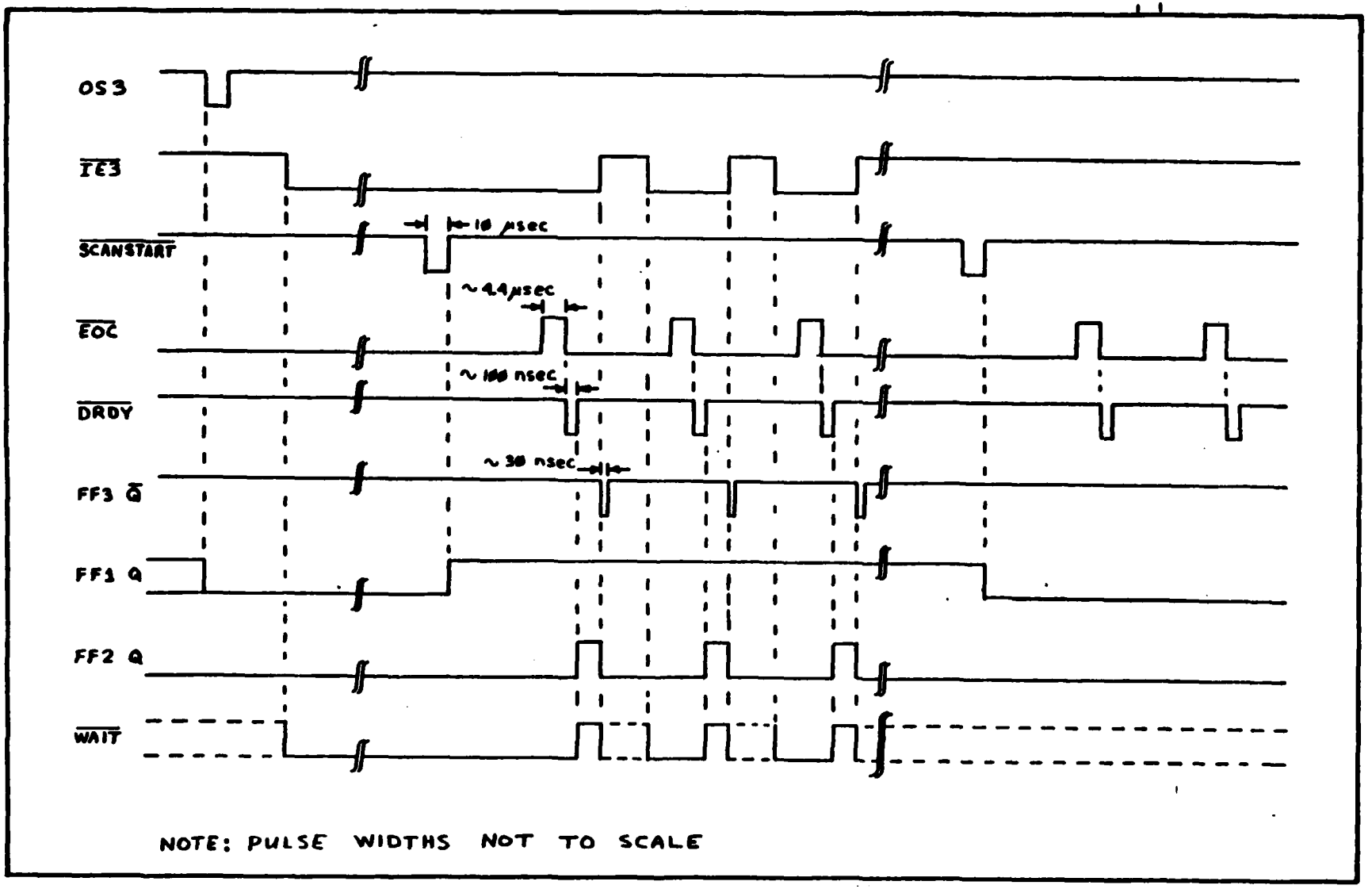


Fig 16. WAIT-State Controller (WSC) Timing Diagram

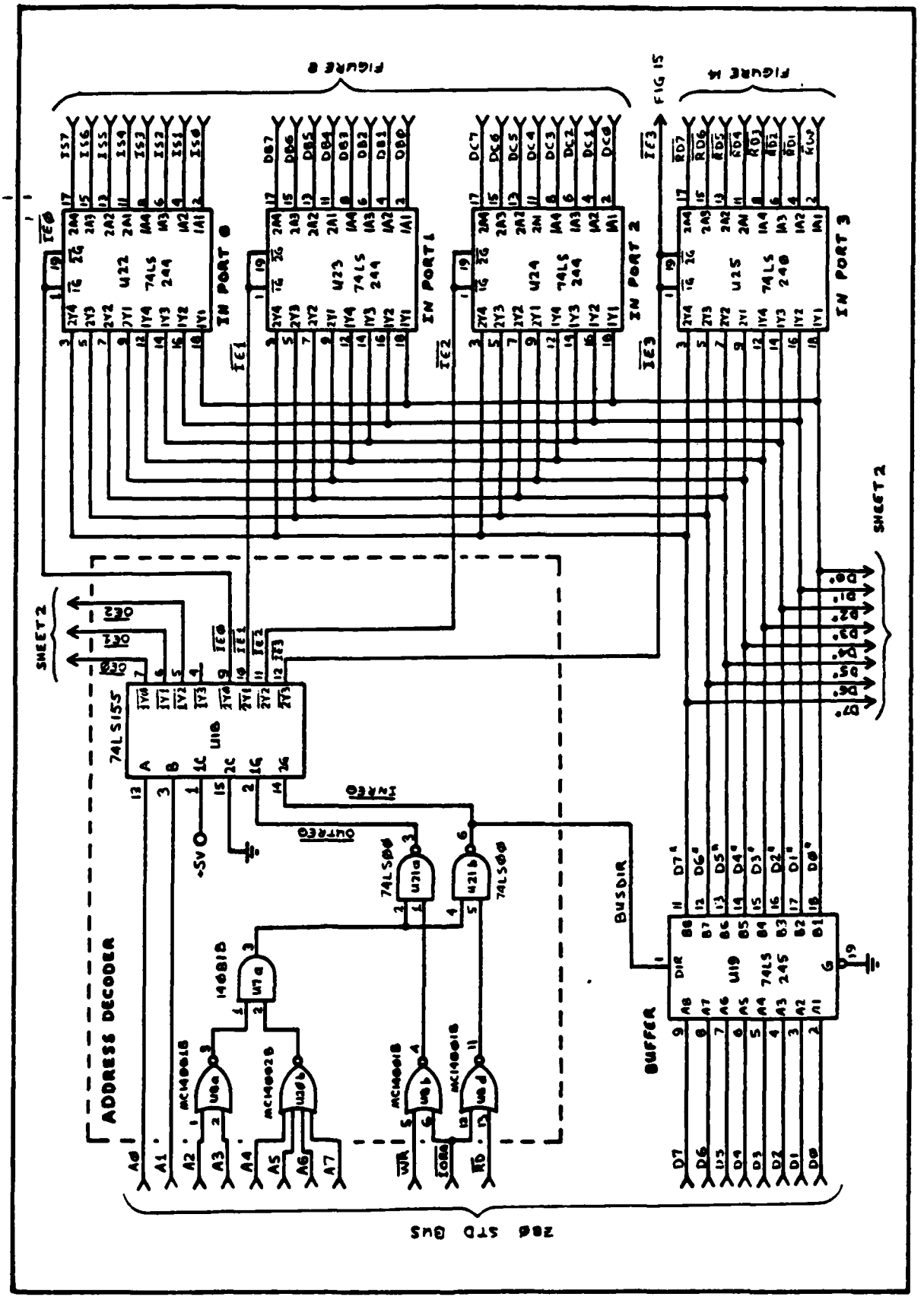


Fig 17. (Sheet 1) Input/Output (I/O) Circuit Schematic

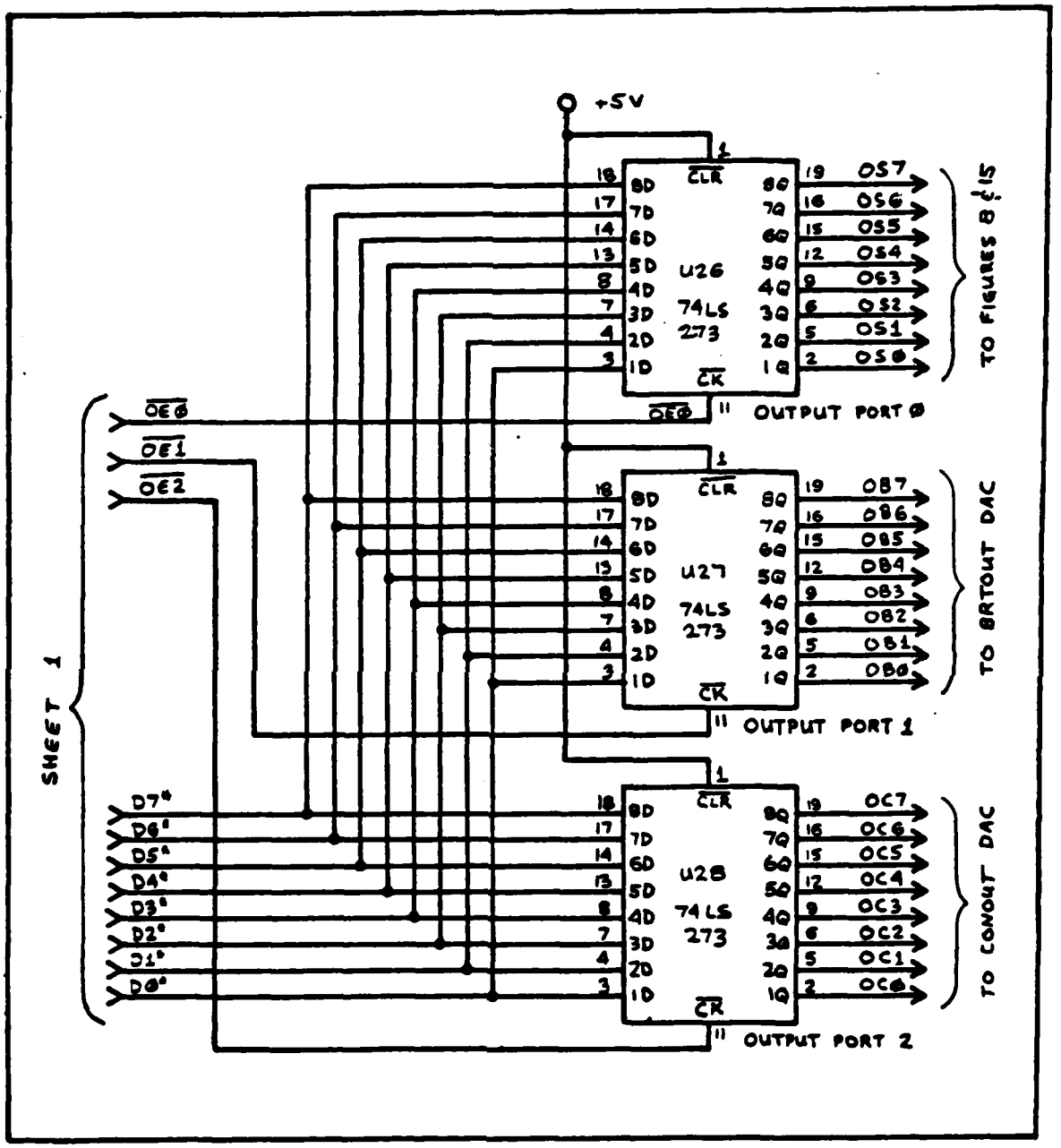


Fig 17. (Sheet 2) Input/Output (I/O) Circuit Schematic

APPENDIX B

COMMERCIAL CIRCUITRY DATA SHEETS

The information contained here includes the commercial technical data for the Reticon circuitry, Mostek MDX-CPU2 microcomputer, luminance processor integrated circuit, and the terminal connections for the Sierracin power supply. In the near future, this data may not be available and is therefore included for future reference.

EG&G RETICON

G SERIES SOLID STATE LINE SCANNERS
128, 256, 512 and 1024 ELEMENTS

The Reticon G-series solid state line scanners are optimized for second-generation solid state image sensor applications. Devices in this series contain 128, 256, 512 or 1024 photodiodes on 25 μm centers. Applications include optical character recognition, pattern recognition, facsimile and non-contact measurement. Key features of these improved devices include:

- **On chip driver and parts of video processing circuit**
- **Simplicity of use—single-phase TTL clock**
- **Several units can be directly cascaded for higher resolution**
- **Differential output for on-chip noise cancellation**
- **Charge storage mode operation for high sensitivity**
- **Standard dual-in-line ceramic package with optical window**

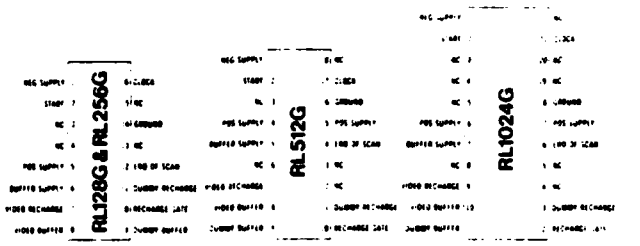


Figure 1. Pin configuration for G-series devices.

The part number RL128G, etc indicates the number of diodes in the various devices. The diodes are on 25 μm centers in all cases. The devices are packaged in 16, 18, or 22 pin dual-in-line integrated circuit packages with ground and polished optical windows.

GENERAL DESCRIPTION

The Reticon "G" series is a family of monolithic self-scanning linear photodiode arrays. The devices in this series consist of a row of silicon photodiodes, each with an associated storage capacitor on which to integrate photocurrent and a multiplex switch for periodic readout via an integrated shift register scanning circuit. The shift register clock driver is also integrated so that only a single-phase TTL clock is required for scanning. A row of dummy diodes is read out differentially with the photodiodes to allow cancellation of multiplex switching transients, and to provide a clean video signal with a minimum of external circuitry. The 512 and 1024 devices are designed for low-cost facsimile applications and can easily be cascaded for extremely high resolution by optically dividing the field of view between two or more devices. The 128 and 256 element devices are well suited for OCR applications. Any of these devices may be used for non-contact measurement and inspection depending on the required resolution.

EQUIVALENT CIRCUIT

A greatly simplified equivalent circuit of a "G" series line scanner is shown in Fig. 2*. Each cell consists of a photodiode and a dummy diode both with an associated storage capacitance. These diodes are connected through MOS multiplex switches to video and dummy recharge lines which are common to all the cells. The switches are sequentially closed for one clock period by the shift register scanning circuit, thereby recharging each cell to 5 volts and storing a charge of approximately 3 pcoul on its capacitance. The scanning circuit is driven by a single-phase TTL clock with a periodic TTL start pulse introduced to initiate each scan. The cell-to-cell sampling rate is the clock frequency, and the total time between line scans is the interval between start pulses. During this line time, the charge stored on each photodiode is gradually removed by photocurrent. The photocurrent is the product of the diode sensitivity and the light intensity or irradiance. The total charge removed from each cell is the product of the photocurrent and the line time. This charge must be replaced through the video line when the diode is sampled and reset once each scan.

In addition to the signal charge, switching transients are capacitively coupled into the video line by the multiplex switches. These same transients are introduced into the dummy line and therefore they can be eliminated and a clean signal recovered by reading out the video and dummy lines differentially.

In many applications, the recharge gate is biased to the negative supply potential and an output signal is obtained simply by differentially amplifying the recharge pulses on the video and dummy recharge lines. However, internal buffer amplifiers are also provided which may be used as part of a sample and hold video output circuit.

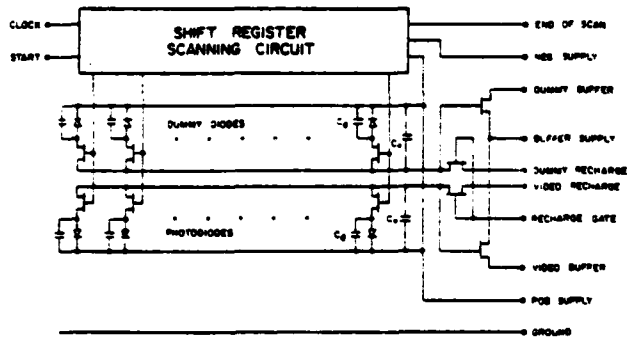


Figure 2. Simplified equivalent circuit for G-series devices.

SENSOR GEOMETRY

In the "G" line scanners the light-sensing area is a long, narrow rectangular region defined by an aperture in an opaque mask. Bar-shaped photodiodes extend across the aperture and are connected to the storage capacitors and multiplex switches buried under the mask. The entire aperture is photosensitive; photocurrent generated by light incident between the photodiodes will be collected by the nearest diode. Figure 3 shows the aperture geometry along with an idealized response function which would be obtained by scanning a point source of visible light along the length of the aperture.

*In the schematic diagram of Fig. 2 the block labeled "shift register scan circuit" consists of two two-phase dynamic shift registers and a drive circuit which generates four clock phases and two properly timed start pulses to load the two registers. The individual cells are actually interdigitated with the odd elements being sampled by one register and the even numbered cells by the other register.

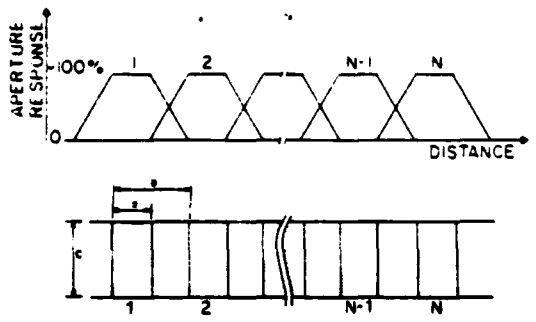


Figure 3. Sensor geometry and idealized aperture response function.

The dimensions a, b and c indicated in Fig. 3 are as follows: the photodiode width *a* is 15 μm, the center-to-center spacing *b* is 25 μm, and the aperture width *c* is 26 μm.

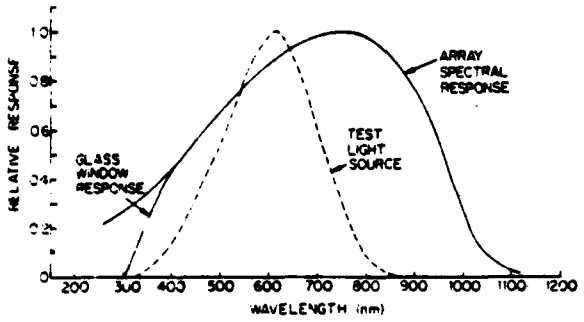


Figure 4. Relative spectral response as a function of wavelength. Dotted line shows spectral distribution of light source used for sensitivity measurements. Quartz and glass windows have similar response except the glass window will fall off at approximately 300 nm as shown above.

SENSITIVITY AND SPECTRAL RESPONSE

The spectral response of the G-series devices is similar to that of other high-quality silicon photodetectors, covering the range from the near UV to the near IR. A glass window is standard, however, an optional quartz window is available. Relative spectral response is shown as a function of wavelength in Fig. 4. Note that relatively high responsivity is maintained even in the blue end of the spectrum because there is no interfering structure covering the diode. As most applications for these devices (OCR, fax, etc.) utilize visible light, the sensitivity and uniformity of response are specified using a source with the spectral distribution shown by the dotted line in Fig. 4. This spectral distribution is produced by filtering a 2870° K tungsten source with a Fish-Schurman HA-11 heat absorbing filter 1 mm thick.

Since Reticon line scanners operate in the charge storage mode, the charge output of each diode (below saturation) is proportional to exposure, i.e., the irradiance or light intensity multiplied by the integration time or the time interval between successive start pulses. Thus, there is an obvious trade-off between scanning speed and the required light intensity. A plot of charge output versus exposure is shown in Fig. 5 for the light source of Fig. 4.

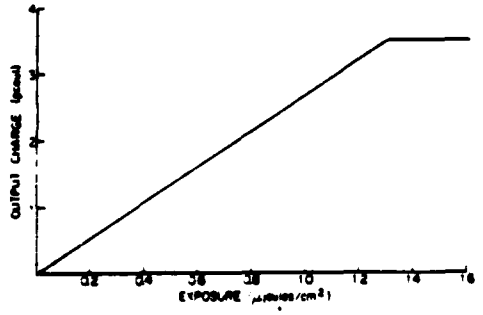


Figure 5. Signal charge per cell as a function of exposure (light intensity x line scan time).

Uniformity of response along the length of a photodiode array is a function of wavelength. Devices tend to be less uniform at long wavelengths (IR) and more uniform at short wavelengths (visible). The non-uniformity specifications of the G-series are based on the light source of Fig. 4.

DARK RESPONSE AND DYNAMIC RANGE

There are three components to the dark output signal from a Reticon line scanner. (1) The integrated dark leakage current—(2) the fixed pattern noise caused by incomplete cancellation of clock switching transients which are capacitively coupled into the video line—and (3) the random pixel noise.

The dark leakage current will vary from element to element but is typically less than 1 pA at room temperature. Assuming this value, leakage current would contribute an output charge of 1 pcoul with a 1 msec line time or .04 pcoul with a 40 msec line time. Thus, since the saturation charge is typically 4 pcoul, dark current will contribute about 1% of the saturated output signal for $t_L = 40$ msec, 0.1% for $t_L = 4$ msec, and so on. The dark current is a very strong function of temperature, approximately doubling every 7°C. Thus the maximum allowable line time becomes correspondingly shorter at high temperatures, and longer at low temperatures. An important feature of the "G" device design is the low power dissipation which means that self-heating is negligible. Dark current does not become a limiting factor in the dynamic range unless very long integration times or highly elevated temperatures are used.

The switching noise appears as a fixed pattern which is spatially random except that it may have a slight 1, 2, 3, 4 pattern because alternate diodes are sampled on different phases of an internally-generated, four-phase clock. Fixed pattern noise is largely removed by differential readout; its residual amplitude will typically be 1% of the saturation level.

Pixel noise is the random, non-repetitive fluctuations which are superimposed on the dark level, and is the ultimate limiting noise which cannot be removed by signal processing. Its rms value will generally be amplifier limited at a value less than about 0.1% of the saturation level, depending on the noise bandwidth and preamplifier used.

The dynamic range that can be achieved depends on circuit complexity and layout techniques. Care must be exercised in circuit layout to provide for adequate ground plane, circuit decoupling, and avoidance of electrostatic pickup.

DRIVE REQUIREMENTS

Two power supplies to the array are required—nominally +5 and −10 volts. The clock and start timing signals may be at TTL level, and may be supplied from other parts of the

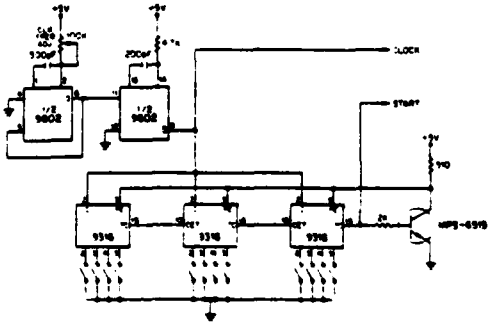


Figure 6. Clock and counter circuit suitable for generating TTL clock and start pulses. The number of clock periods between start pulses may be set at any value up to 4096 by setting the switches.

system or generated by using a simple circuit such as that shown in Fig. 6. In this circuit, the start pulse is obtained by counting clock pulses. By setting the appropriate switches, the number of clock periods n, between start pulses may be set at any desired value greater than or equal to N, the number of elements in the array. However, the total time between starts pulses $t_L = n/f_S$ should not exceed approximately 40 msec (at room temperature) to prevent integrated dark current from making a significant contribution to the output charge.

A timing diagram showing the relationships between the clock and start pulses and the video and end-of-line outputs is shown in Fig. 7.

SIGNAL EXTRACTION

The video output of the "G" devices is a train of N charge pulses flowing onto the video recharge line and dummy recharge line capacitances during each scan, with timing as shown in Fig. 7. The pulses on the dummy line contain

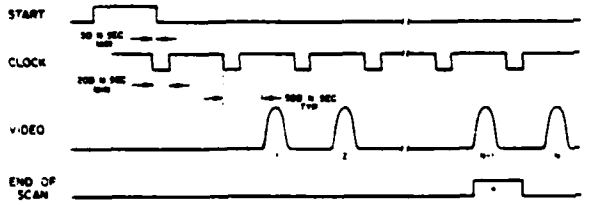


Figure 7. Timing diagram showing relationship of clock and start inputs to video and end-of-scan outputs.

switching transients only; those on the video line contain switching transients plus the video signal. An output circuit is required which is capable of differentially amplifying these pulses to a useable voltage level. Two types of amplifier circuits are in common use—1 a simple differential current amplifier—and 2 a video line integration, sample-and-hold circuit. The former has a pulse output while the latter has a boxcar output waveform.

CURRENT AMPLIFIER.

A simple differential current amplifier circuit is shown in Fig. 8. In this mode of operation, the recharge gate is

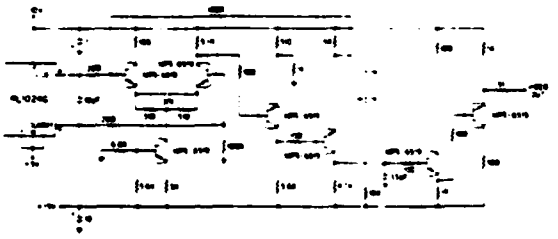


Figure 8. Differential current amplifier circuit for RL-1024G.

biased ON by connecting it to the negative supply and the signal is obtained through the video dummy and recharge lines. The unused buffer amplifiers are biased OFF by connecting all pins to the positive supply. An example of the video output of the circuit of Fig. 8 is shown in the oscilloscope photograph of Fig. 9.

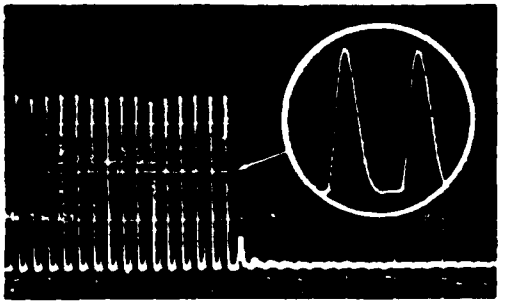


Figure 9. Oscilloscope photograph showing video output of circuit of Fig. 8.

INTEGRATE, SAMPLE-AND-HOLD AMPLIFIER. This alternative signal processing scheme makes use of the internal buffer amplifiers and recharge switches. Immediately after the multiplex switch is closed to sample a diode, the voltage change on the video line is sensed through the buffer amplifier, and sampled and held. The recharge gate is then pulsed negative to reset the video line before the next diode is sampled. The result is a sampled and held boxcar video signal such as that shown in Fig. 10.

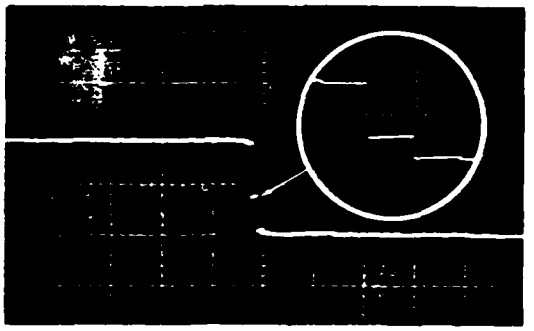


Figure 10. Oscilloscope photograph showing video output of integrate, sample-and-hold amplifier.

END-OF-SCAN

An output pulse is provided when the next-to-last element is sampled by the shift register scanning circuit. This end-of-scan output is provided primarily for test purposes. When not in use, it should be connected to the positive supply to avoid introduction of unwanted "glitches" into the video. In some applications, however, it may be desirable to use the end-of-scan output. In these cases, it is recommended that the voltage excursion on the end-of-scan terminal be minimized by using a circuit such as that shown in Fig. 11. This figure shows a common application

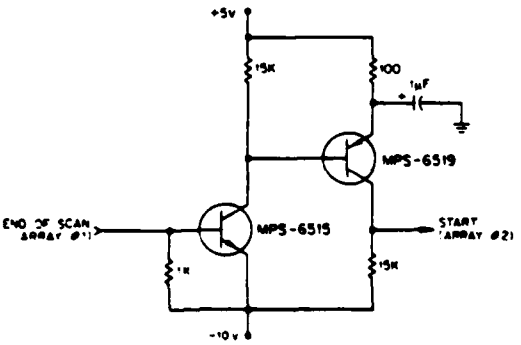


Figure 11. End-of-scan output circuit suitable for generating start pulse for a second array.

in which the end-of-scan output of one array is used to generate the start pulse for a second array. The timing is such that the last element of the first array and the first element of the second array are sampled on successive clock pulses.

CIRCUIT CARDS

Printed circuit cards containing all required drive and amplifier circuitry for operation of the "G" series self-scanning photodiode arrays are available from Reticon. These circuits are highly recommended for first-time array evaluation. In many cases they are also useful for design into final equipment.

Two families of circuit cards are available, corresponding to the two amplifier configurations described earlier. Both circuits are complete except for power supplies and have the flexibility to operate over a wide range of scan rates and integration times.

RC300 SERIES. These boards incorporate the clock and counter circuit of Fig. 6 and the amplifier circuit of Fig. 8. They provide a pulse type output such as that shown in Fig. 9 and give good performance at lowest cost. The boards are 3 inches square, and have mounting holes in each corner on 2.6-inch centers. An example is shown in Fig. 12.

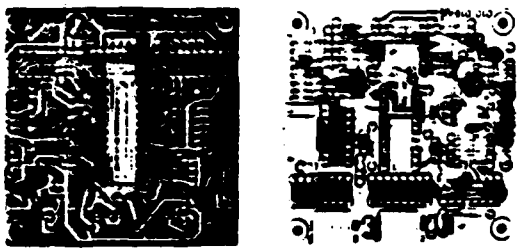


Figure 12. RC303 circuit card with RL1024G array.

RC100B SERIES. These circuits provide an integrated, sampled-and-held boxcar output such as that shown in Fig. 10. They are recommended for high-performance applications which require this output waveform. Each circuit is divided into two boards—a standard "motherboard" which contains most of the circuitry, and a small "array board" which contains only those components which must be located close to the array. The array board may be plugged directly into the motherboard or can be extended up to 30 inches away via an optional ribbon cable.

The motherboard (RC100B) is 4.5 x 6.5 inches in size and is terminated by a standard 22-pin edge connector. The array boards (RC104, etc.) are 3 inches square and have mounting holes in each corner on 2.6-inch centers. A different array board is required for each array type:

Photodiode Array	*Current Amplifier Circuit*	*Sample and Hold Circuit*
RL-128G	RC301	RC100/104
RL-256G	RC301	RC100/104
RL-512G	RC302	RC100/105
RL-1024G	RC303	RC100/106

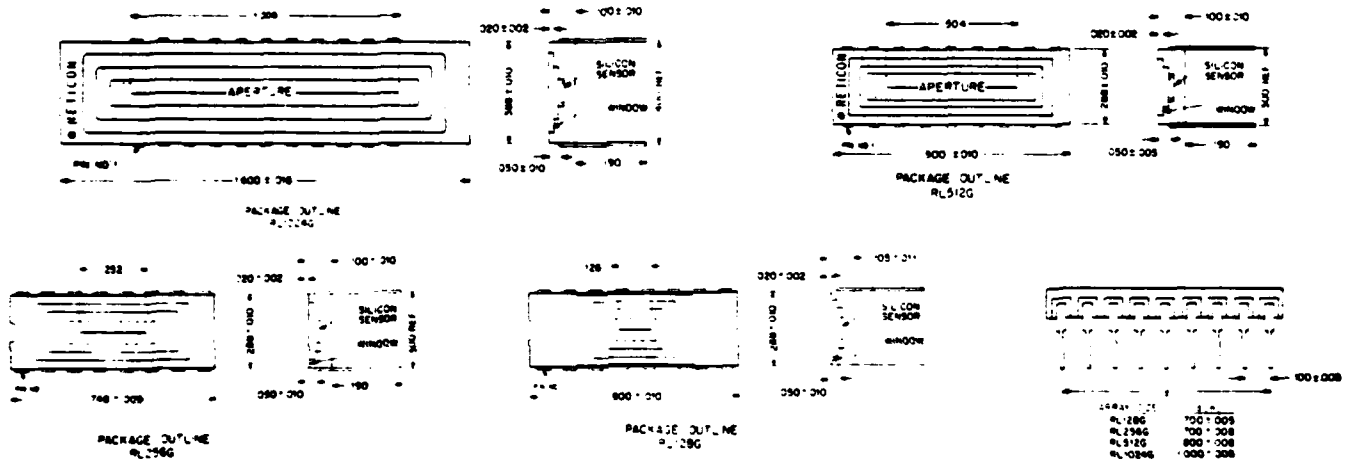


Figure 13. Outline drawing of G-series devices.

SPECIFICATIONS

ELECTRICAL CHARACTERISTICS (25° C)

		Min	Typ	Max	Units
1	Positive Supply Voltage Vp	+4.5	+5	+5.5	volts
	Negative Supply Voltage Vn	−10.5	−10	−9.5	volts
	Clock Voltage Low Vcl	−10.5	0	+1	volts
	Clock Voltage High Vch	Vp − 1	+5	Vp	volts
	Start Voltage Low Vsl	−10.5	0	+1	volts
	Start Voltage High Vsh	Vp − 1	+5	Vp	volts
	Recharge Gate Voltage Low VRL	−10.5	−10	−9.5	volts
	Recharge Gate Voltage Low VRH	Vp − 1	+5	Vp	volts
	Clock Pulse Width	0.2	—	—	usec
	Start Pulse Width		See Fig. 7		
	Clock Frequency fc	—	—	1	MHz
4	Integration Time ti	—	—	40	msec
4.2	Clock Input Capacitance Cc	—	4	—	pF
4.2	Start Input Capacitance Cs	—	4	—	pF
4.2	Video Line Capacitance Cv				
	RL-1024G	—	30	—	pF
	RL-512G	—	20	—	pF
	RL-256G	—	12	—	pF
	RL-128G	—	8	—	pF
	End-of-Scan Output Resistance	—	5	—	Kohm
	D-C Power Dissipation	—	45	—	mwatts

ELECTRO-OPTICAL CHARACTERISTICS (25° C)

		Min	Typ	Max	Units
	Diode Center-to-Center Spacing	—	25	—	μm
	Diode Aperature Width	—	26	—	μm
4,3	Photodiode Sensitivity	—	2.5	—	pA/μwatt/cm2
4,3	Non-uniformity of Sensitivity				
	RL-128G	—	7	10	±%
	RL-256G	—	7	10	±%
	RL-512G	—	9	11	±%
	RL-1024G	—	12	14	±%
4,3	Saturation Exposure	—	1.8	—	μjoules/cm2
4	Saturation Charge	—	4	—	pcoul

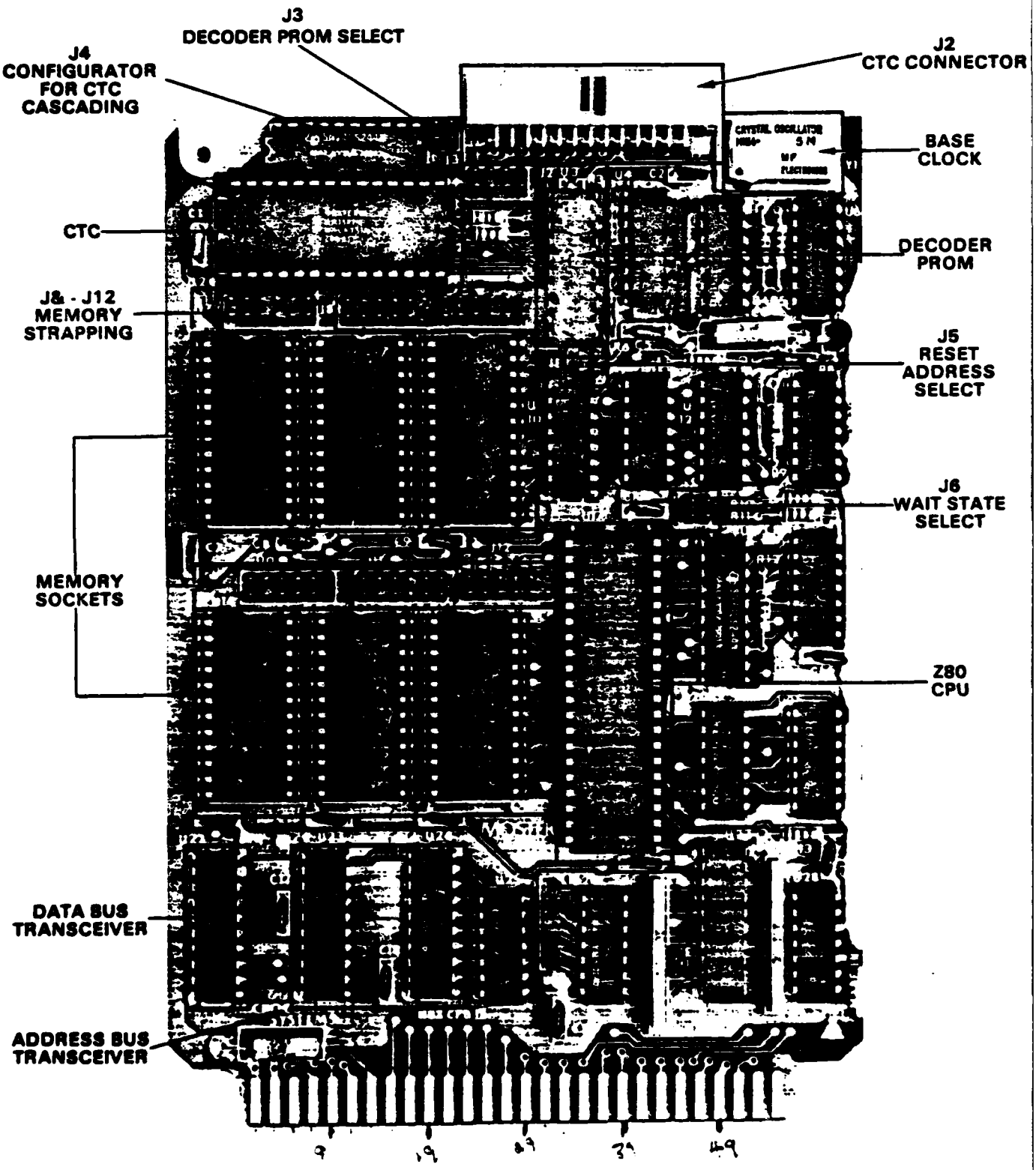
ABSOLUTE MAXIMUM RATINGS

	Min	Max	Units
Voltage on Any Terminal	Vp - 20	Vp	volts
Storage Temperature	-55	+125	°C
Temperature Under Bias	-55	+85	°C

NOTES:

1. No terminal should ever be allowed to go more positive than Vp
2. Measured with nominal power supply voltages
3. Measured using light source of Fig. 4 neglecting first 2 and last 2 diodes
4. July 1981 revision, no change of design

FIGURE 1-1 MDX-CPU2 BOARD PHOTO



SECTION 2.0

FUNCTIONAL HARDWARE DESCRIPTION

2.1 INTRODUCTION

The MDX-CPU2 utilizes the MK3880 (Z80) microprocessor as the system controller. It features six 24-pin memory sockets which enable the user to populate the module with any combination of designated ROM, RAM and EPROM. Flexible address decoding allows the user to configure each memory device within any 1k boundary of the 64k memory map. A PROM decoder is supplied which will allow the user to choose one of four popular memory configurations, or, if desired, the user may implement any possible mixture of memory devices simply by programming a decoder PROM accordingly. A programming example is shown in Appendix E.

Address, data and control busses have been made bidirectional to allow external DMA Controllers to directly access on-board memory.

A 4-channel counter/timer circuit (MK 3882) is included on-board for software controlled counting and timing functions. The CTC Trigger inputs and Zero Count outputs are buffered and brought out to a connector for external access. In addition, an on-board strapping option makes it possible to cascade the four CTC channels for long count sequences.

Another strapping option allows the user to select a reset address of either 0000H or E000H. The E000 option is required for use of standard MOSTEK software and hardware products including DDT-80, ASMB-80, FLP-80DOS/MDX, MDX-SST, and MDX-DEBUG. These products also require strapping on-board RAM to reside at Location FC00 through FFFF so that it will act as the operating system RAM for DDT-80.

A 4 MHZ version of MDX-CPU2 is also available (MDX-CPU2-4). In this version a jumper option enables automatic insertion of one WAIT state during on-board memory cycles for those memory devices having access times greater than 250 ns.

The decoder PROM supplied is programmed to identify MK2716 EPROMs as "slow" and MK4118 STATIC RAMs as "fast"; i.e., wait states will not be generated for MK4118 devices.

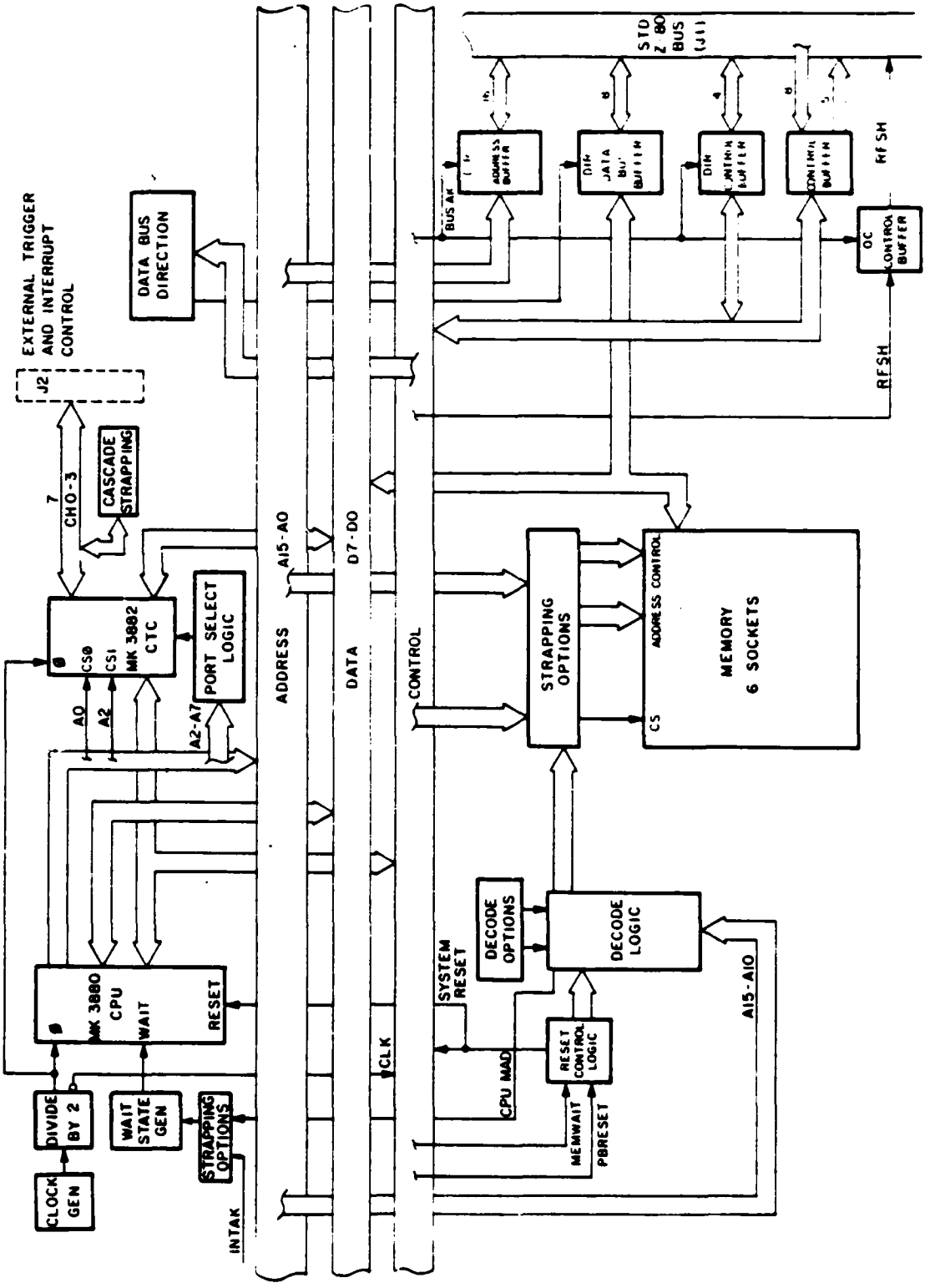
2.2 BLOCK DIAGRAM DESCRIPTION

Figure 2-1 is a block diagram illustrating the flow of system address, data and control signals on MDX-CPU2. The following paragraphs describe the function of each of the major blocks.

2.2.1 CPU.

The MK3880 (Z80) CPU is the system controller. It fetches, decodes and executes instructions from memory and generates the necessary address and control signals to coordinate data flow between the CPU and memory, or between the CPU and system I/O devices. Refer to the MK3880 Technical Manual for a complete description of the MK3880 CPU.

FIGURE 2-1 MDX-CPU2 BLOCK DIAGRAM



2.2.2 CLOCK GENERATOR

A hybrid, crystal-controlled oscillator generates the basic clock signals necessary for sequencing and synchronizing all CPU operations. The divide-by-2 block ensures a 50% duty cycle. The system clock frequency is 2.5 MHZ for MDX-CPU2 and 4.0 MHZ for MDX-CPU2-4. An inverted clock is applied to the system bus for use by other modules.

2.2.3 CTC (COUNTER/TIMER CIRCUIT)

The MK3882 Counter/Timer Circuit provides four independent, programmable channels for either software or hardware controlled counting and timing functions. Each channel can be configured by the CPU for various modes of operation and the built-in daisy chain priority interrupt logic provides for automatic, independent interrupt vectoring. The I/O port addresses for the CTC are hard-wired as follows:

I/O PORT ADDRESS	CTC CHANNEL
7C	0
7D	1
7E	2
7F	3

The Trigger inputs and Zero Count outputs are buffered and brought out to a connector for external hadware control. A strapping option has also been included to permit any or all of the four CTC channels to be cascaded for long count sequences.

Section 3 provides the necessary information for utilizing this option. For a complete description of CTC operation, refer to the MK3882 Technical Manual.

2.2.4 MEMORY

The MDX-CPU2 has been designed to accommodate any combination of the above

mentioned RAM, ROM and EPROM devices. Six 24-pin sockets have been provided, each of which may be strapped for any of the allowable memory types and for any 1k address boundary within the 64K Z80 memory map. These user-selectable options are fully described in Section 3.

2.2.5 DECODE LOGIC

This section primarily consists of a 256x8 PROM which decodes the high order six bits of memory address and generates the applicable chip select if on-board memory is to be selected. The 256 byte PROM provides for four separate memory configurations and is supplied programmed as defined in Section 3 and Appendix E. A strapping option must be hard-wired to the desired configuration as explained in Section 3.

2.2.6 RESET CONTROL LOGIC

This is a strapping option that causes a hardware-forced memory starting address upon system reset. A reset address of either 0000H or E000H may be selected.

This logic is required for use of standard MOSTEK hardware and software products including DDT-80, FLP-80DOS/MDX, MDX-SST, and MDX-DEBUG.

2.2.7 WAIT STATE GENERATOR

This function, if selected, causes on-board memory read and write cycles to be lengthened by one clock period in order to allow sufficient access time when slower memory devices are used. Each socket is selected independently for wait state generation as determined by the decoder PROM firmware. The decoder PROM supplied is programmed to cause a wait state to be inserted whenever on-board 2716 EPROMs are addressed. No wait states are generated during 4118 RAM access. This option should only be necessary for 4 MHZ CPU operation. The wait state generator for on-board memory may be disabled by disconnecting J6 pins 1 and 2.

The wait state generator may also be strapped to insert an additional wait cycle during interrupt acknowledge. The use of this option is dependent on the CPU clock frequency and the number of interrupting devices in the daisy chain. It is enabled by connecting J6 pins 3 and 4.

CA3144G

TV Luminance Processor

The CA3144G is a monolithic silicon integrated circuit that performs the luminance processing functions of amplification; contrast, brightness and peaking control; blanking; and black-level clamping.

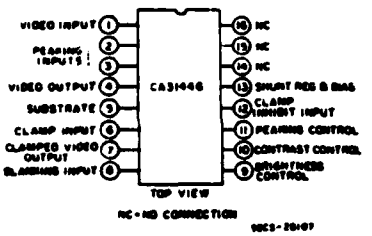
This device, when used in conjunction with the CA3126Q chroma processor and the CA3137E chroma demodulator, will provide a luminance/chrominance system having excellent tracking of controls. The CA3144G is supplied in a 16-lead hermetic Gold-CHIP dual-in-line plastic package ("G" suffix).

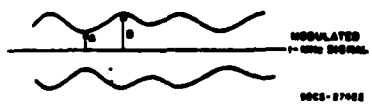
The semiconductor junctions in this device are sealed by utilizing a silicon nitride passivation layer. A multi-layered, highly corrosion-resistant, terminal-connection system of unique design is employed.

Features:

- Black-level clamping
- Linear dc controls for brightness, contrast, and peaking
- Horizontal and vertical blanking
- "Hermetic Chip" construction
- Silicon nitride passivated
- Platinum silicide ohmic contacts
- Gold-CHIP metallization
- Operates with standard or tapped delay line

TERMINAL ASSIGNMENT





A = Amplitude of 50-kHz signal at deepest trough
B = Peak amplitude of 50-kHz signal

$$\text{Downward Modulation} = \frac{B-A}{B}$$

MAXIMUM RATINGS, *Absolute-Maximum Values:*

DC SUPPLY CURRENT (into Terminal 13)* . . . . . 57 mA

DEVICE DISSIPATION: *
- Up to T_A = 55°C . . . . . 750 mW
- Above T_A = 55°C . . . . . derate linearly 7.9 mW/°C

AMBIENT-TEMPERATURE RANGE:
- Operating . . . . . −40 to +85°C
- Storage . . . . . −65 to +150°C

LEAD TEMPERATURE (During soldering):
- At distance 1/16 ± 1/32 inch (1.59 ± 0.79 mm) from case for 10 s max. . . . . +265°C

* Although the CA3144G is rated for maximum dissipation of 750 mW, it is recommended that the current into terminal 13 be limited by external circuit resistance to 30 mA for a typical voltage at terminal 13 of 12.3 volts.

ELECTRICAL CHARACTERISTICS at T_A = 25°C

Characteristic	Bias Volts (V)	Test Conditions: Switch Numbers S1 S2 S3 S4 S5 S6 S7 S8 S9 S10 S11 — Switch Positions For Characteristics Measurements											LIMITS Min.	Typ.	Max.	UNITS
STATIC																
Voltage: At Term. 13 (V13)	6.5	2	1	1	2	2	4	1	2	2	1	1	11	12.3	13.2	V
Quiescent Voltage At Term. 4 (V4)	6.5	2	1	1	2	2	3	1	2	2	1	1	3.3	4	5.7	V
Quiescent Voltage At Term. 7 (V7)	6.5	2	1	1	2	2	2	1	2	2	1	1	7.1	7.7	8.3	V
Current into Term.13 (Term.13 Connected to +11 V) (I13)	6.5	2	1	1	2	2	3	1	2	2	1	2	10	18	30	mA
DYNAMIC																
Wide-Band Gain (Note 1)	7.3	1	1	1	2	1	2	1	1	1	2	1	1	3	5	dB
Contrast Gain Reduction (Note 2)	7.3	1	1	1	2	1	2	1	1	2	2	1	27	30	-	dB
Peaking Gain (Note 1)	7.3	1	1	2	2	1	2	1	1	1	2	1	9	13	17	dB
Peaking Gain Reduction (Note 3)	7.3	1	1	2	2	1	2	1	1	1	2	1	16	18	-	dB
Max. Intermodulation Distortion: 3.8 V (Note 4)	7.3	1	-	1	1	1	2	-	2	1	2	1	-	20	-	%
5 V (Note 5)	7.3	1	-	1	1	1	2	-	2	1	2	1	-	40	-	%

Note 1:
Set 50-kHz generator for 200 mV_{rms}. Adjust R1 peaking control for minimum setting (see Fig. 2). Measure wide-band gain at terminal 7.

Note 2:
Set 50-kHz generator for 200 mV_{rms}. Adjust R1 for minimum setting. Measure contrast gain reduction at terminal 7.

Note 3:
Set 50-kHz generator for 200 mV_{rms}. Adjust R1 for maximum setting. Measure peaking gain reduction at terminal 7.

Note 4:
Adjust R1 for minimum setting. With S2 at switch position 1 and S7 at switch position 3, set 50-kHz generator for 3.8 V_{p-p}. Then with S2 at switch position 2, set 1-MHz generator for 200 mV_{rms}. Then with S7 at switch position 2, measure downward modulation of the 1-MHz signal due to the 50-kHz signal.

Note 5:
Repeat step 4 except that the 50-kHz generator must be set at 5 V_{p-p}.

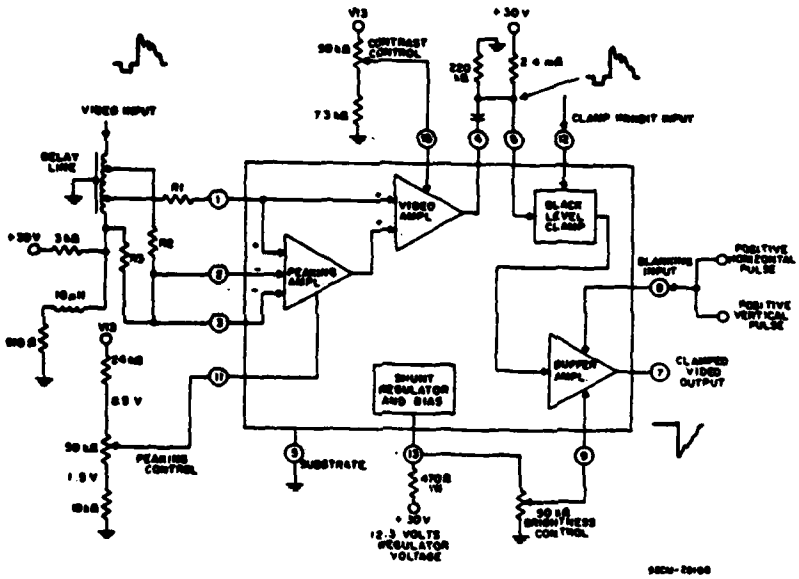


Fig. 1 – Functional block diagram.

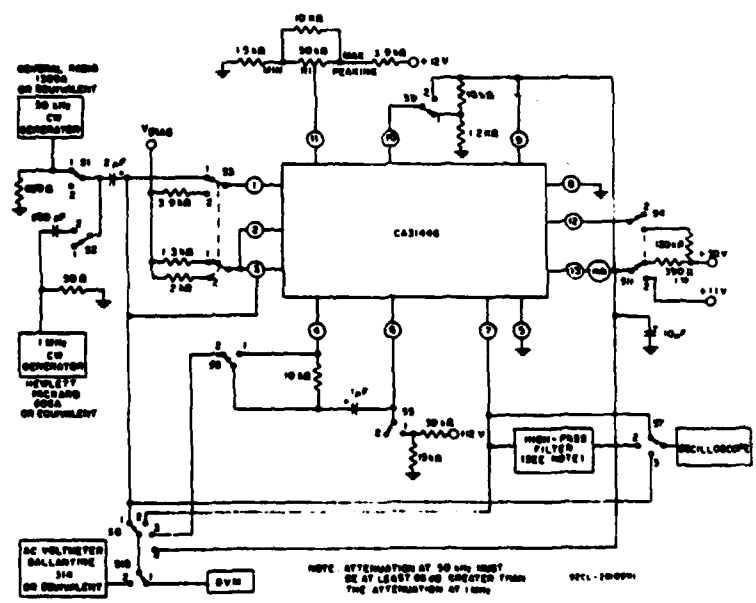


Fig. 2– Test circuit.

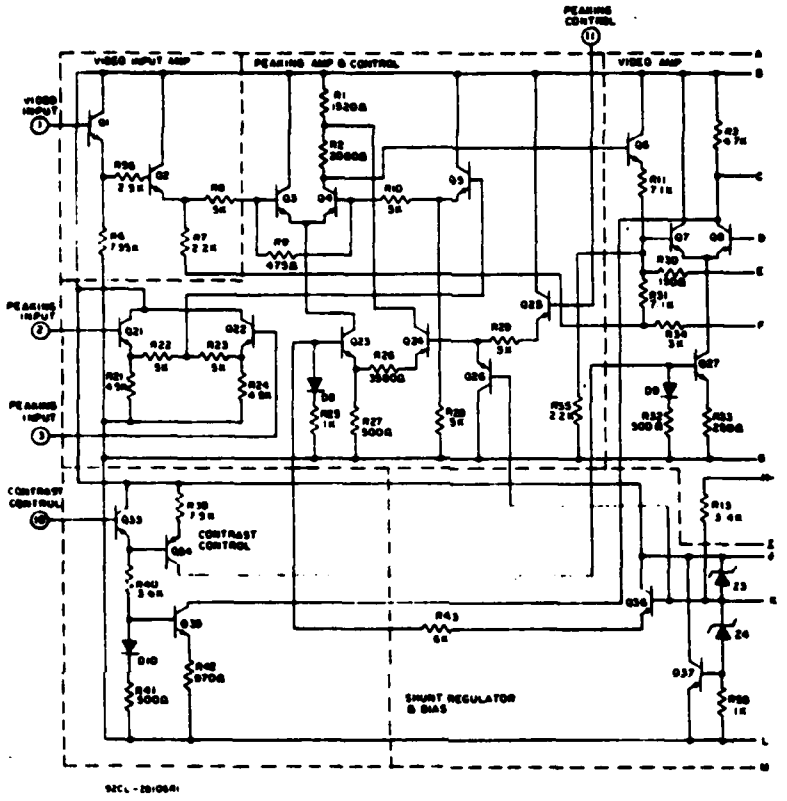


Fig. 3 – Schematic diagram

CIRCUIT DESCRIPTION

Fig. 1 is a block diagram of the CA3144G indicating the internal functions as well as external circuitry and signals. The video input signal with negative-going sync is applied to the input of the tapped delay line. Signals from fixed taps of the delay line are applied to terminals 1, 2, and 3 of the CA-3144G. In referring to Fig. 4, the signal from the delay line tap A is applied to the video input at terminal 1. The signals from taps B and C are summed where $V_A + V_B = V_{sum}$. The signal (V_{sum}) is then applied to the parallel connection of the peaking input terminals, 2 and 3. The video input signal is applied to a non-inverting input of the peaking amplifier while the peaking input signal (V_{sum}) is applied to an inverting input of the peaking amplifier.

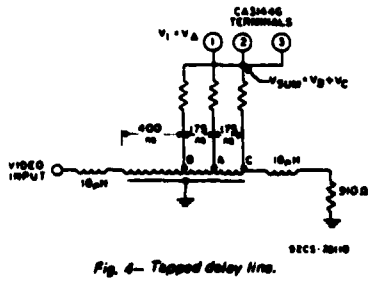


Fig. 4– Tapped delay line.

Low-frequency video components are unattenuated, while high-frequency components are attenuated as a function of the delay-line tap points. The peaking amplifier is a differential amplifier, so that the output is proportional to V_1 minus V_{sum}. At low frequencies, the signal at terminals 2 and 3 is unattenuated, and the peaking amplifier produces no output at these frequencies. However, at high frequencies the signal at ter-

B-14

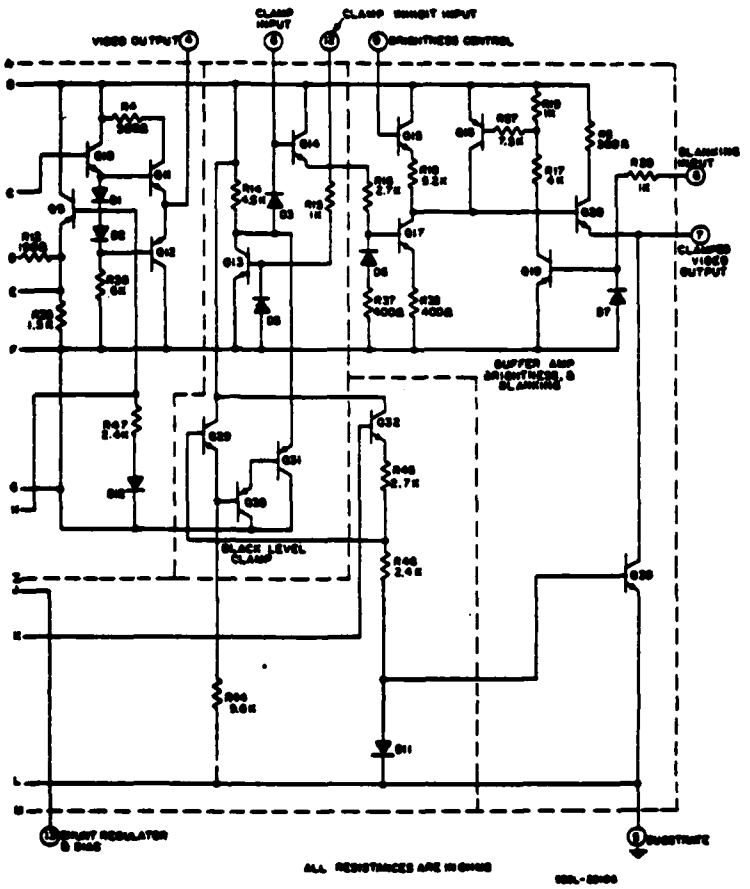
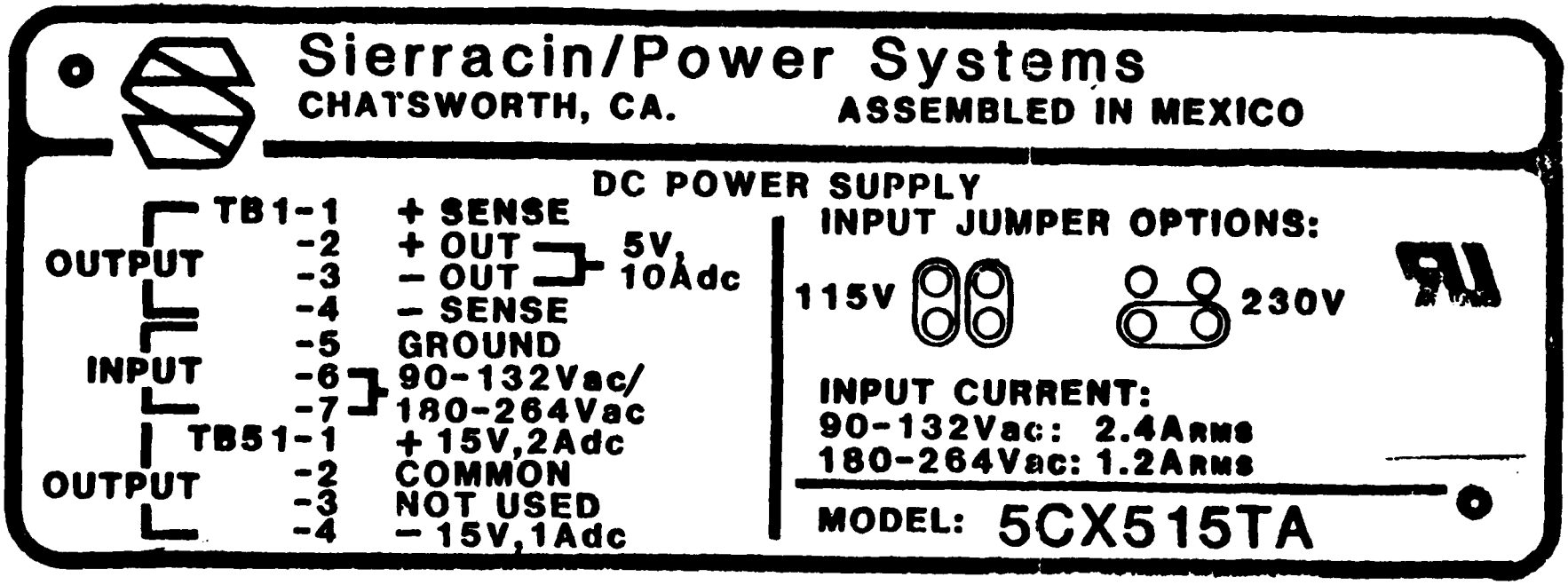


Fig. 3— Schematic diagram

minals 2 and 3 is attenuated thus, the peaking amplifier output consists of high-frequency video. The peaking control setting determines the amplitude of the peaking signal which is then fed to the video amplifier, where it is added to the video input signal and amplified. The setting of the peaking control does not substantially affect the dc quiescent voltage at terminal 4.

The low-impedance video amplifier output is at terminal 4. The signal is fed through an external coupling capacitor to terminal 6, the black-level clamp input. The action of the black-level clamp is such that it clamps to the black level rather than to the sync level. Refer to the circuit diagram in Fig. 1. Consider the situation where no signal is applied to terminal 12. Terminal 6 is biased through diode D3. The signal at terminal 6 will clamp its most negative excursion (sync pulse) to the anode voltage of D3. However, if a positive pulse is applied to terminal 12 during the sync interval, the anode of D3 is forced to ground due to saturation of Q13. The clamp is thus disabled, and terminal 6 will clamp to the next lower signal level, the black level.

The clamped video signal at terminal 6 is amplified and inverted at terminal 7. Blanking is accomplished by applying horizontal and vertical sync pulses to terminal 8. The pulses turn ON p-n-p transistor Q18 which shorts the base of transistor Q20 to the terminal 13 supply voltage. The brightness control function is accomplished by varying the voltage on terminal 9. The gain of the inverter stage remains constant, but the dc reference voltage follows the terminal 9 voltage. The contrast control function is accomplished by varying the voltage of terminal 10. Increasing the voltage on terminal 10 lowers the gain of the video amplifier. This reduction in gain does not substantially affect the dc quiescent voltage at terminal 4.



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APPENDIX C

D/A CONVERTER PLOT DATA

Tables C-1, C-2, and C-3 contain the data which was recorded to construct the plots contained in Chapter III. Two separate tables contain data for the brightness D/A converter voltage output vs. luminance output of the video monitor. The third table contains the data gathered for the contrast D/A converter vs. video output while inputting a 4-volt, positive-going 15 KHz pulse to the video amplifier portion of the luminance processor.

TABLE C-1

BRIGHTNESS D/A VOLTAGE OUTPUT vs. VIDEO MONITOR LUMINANCE 1

D/A OUTPUT (V)	LUMINANCE (fL)
1.10	.0009
1.25	.0009
1.40	.0010
1.56	.0011
1.72	.0015
1.88	.0039
2.04	.0093
2.19	.0244
2.35	.06
2.50	.124
2.66	.221
2.82	.335
2.98	.5
3.13	.706
3.29	.95
3.45	1.236
3.60	1.55
3.76	1.86
3.92	2.25
4.07	3.15
4.39	3.65
4.55	4.15
4.71	4.68
4.86	5.28
5.01	5.94
5.18	6.5
5.33	7.11
5.50	7.66
5.66	7.92
5.82	8.34
5.98	8.82
6.14	9.25
6.30	9.87
6.46	10.39
6.62	10.97
6.78	11.54
6.94	12.14
7.10	12.76
7.26	13.35
7.42	14.14
7.57	14.78
7.73	15.40
7.90	16.05
8.05	16.70
8.21	17.50
8.37	18.20
8.53	18.70

8.68	19.3
8.84	20.2
9.00	20.8
9.16	21.5
9.32	22.4
9.47	23.0
9.63	23.8
9.78	24.5
9.94	25.3
10.05	26.1

TABLE C-2

BRIGHTNESS D/A VOLTAGE OUTPUT vs. VIDEO MONITOR LUMINANCE 2

D/A OUTPUT (V)	LUMINANCE (fL)
1.10	1.201
1.25	1.52
1.40	1.874
1.56	2.27
1.72	2.71
1.88	3.21
2.04	3.71
2.19	4.21
2.35	4.74
2.50	5.32
2.66	5.89
2.82	6.50
2.98	7.14
3.13	7.90
3.29	8.69
3.45	9.37
3.60	10.05
3.76	10.71
3.92	11.45
4.07	12.14
4.23	12.85
4.39	13.6
4.55	14.41
4.71	15.23
4.86	16.02
5.01	16.5
5.18	17.3
5.33	18.1
5.49	18.9
5.65	19.7
5.81	20.5
5.96	21.3
6.12	22.0
6.28	22.8
6.43	23.5
6.60	24.2
6.76	25.0
6.91	25.6
7.07	26.0
7.24	26.5
7.40	27.1
7.55	27.6
7.72	28.2
7.88	28.9
8.03	29.4
8.19	30.1
8.35	30.6

8.51	31.3
8.67	31.9
8.82	32.6
8.99	33.5
9.14	33.8
9.30	34.4
9.46	35.0
9.62	35.7
9.78	36.4
9.93	37.1
10.04	37.6

TABLE C-3

CONTRAST D/A VOLTAGE OUTPUT vs. VIDEO AMPLIFIER OUTPUT

D/A OUTPUT (V)	VID. AMP. OUTPUT (V)
0.00	0
.11	0
.27	.03
.42	.06
.58	.08
.74	.10
.89	.12
1.05	.14
1.21	.17
1.36	.19
1.52	.21
1.68	.23
1.84	.25
1.99	.27
2.15	.29
2.31	.31
2.46	.33
2.62	.35
2.78	.37
2.94	.39
3.09	.41
3.25	.45
3.56	.47
3.72	.49
3.88	.51
4.04	.53
4.19	.55
4.35	.57
4.51	.59
4.66	.61
4.82	.63
4.98	.65
5.13	.67
5.29	.68
5.45	.70
5.61	.72
5.76	.74
5.92	.76
6.08	.78
6.24	.80
6.39	.82
6.55	.84
6.71	.86
6.86	.88
7.02	.90
7.18	.90
7.34	.92

7.49	.94
7.65	.95
7.81	.97
7.96	.98
8.12	1.00
8.27	1.02
8.43	1.03
8.59	1.05
8.75	1.06
8.91	1.08
9.06	1.10
9.22	1.12
9.38	1.13
9.53	1.14
9.69	1.15
9.85	1.17
10.0	1.18

APPENDIX D

ASSEMBLY LANGUAGE LISTING

This appendix contains the source listings of the software routines for the sine-wave grating controller described in Chapter IV. The modifications described in Chapter IV have been incorporated in this set of program listings.

```
 .Z80
        CSEG
;FILENAME: PROG2.MAC
;TITLE:   SINE-WAVE GRATING CONTROL ROUTINE
;AUTHOR: ORIGINAL BY CAPT B D BAXLEY, GE-83M
;         MODIFIED BY MARK H. SWANN, GE-83D
;DATE:    31 AUG 83
;SYSTEM: MOSTEK MDX-CPU2
;DESCRIPTION:    THIS PROGRAM IS THE CONTROL SOFTWARE FOR THE
;                SINE-WAVE GRATING CONTROLLER, MODIFIED FOR
;                CALCULATIONS UTILIZING 128 RETICON PHOTODIODE
;                SAMPLES INSTEAD OF 512.
;OPERATION:      THE ROUTINES IN THIS PACKAGE HAVE BEEN SET
;                UP TO RUN AS SOON AS THE MDX-CPU2 IS
;                POWERED UP OR RESET (NOTE: THE MDX-CPU2 MUST
;                BE HARD-WIRED TO BEGIN EXECUTION AT 0000H).
;                ONCE RESET, THIS PROGRAM WILL INITIALIZE THE
;                HARDWARE AND JUMP INTO AN INFINITE CONTROL LOOP.

;****************** CONSTANTS ****************************************

;  MISCELLANEOUS

BBIT     EQU      00H      ;BRIGHTNESS BIT OF STATUS PORTS
CBIT     EQU      01H      ;CONTRAST BIT OF STATUS PORTS
PBIT     EQU      02H      ;PRESET STATUS PORTS BIT
WTBIT    EQU      03H      ;RESET WAIT STATE CONTROLLER BIT
DBSF     EQU      40D      ;DESIRED BRIGHTNESS SCALE FACTOR
DCSF     EQU      100D     ;DESIRED CONTRAST SCALE FACTOR
SCRTCH   EQU      0F800H   ;BEGINNING OF RAM SCRATCH PAD AREA
STACK    EQU      0FC00H   ;TOP OF STACK

;  PORT NUMBERS

ISPORT   EQU      00H      ;INPUT STATUS PORT
OSPORT   EQU      00H      ;OUTPUT STATUS PORT
IBPORT   EQU      01H      ;INPUT BRIGHTNESS PORT
OBPORT   EQU      01H      ;OUTPUT BRIGHTNESS PORT
ICPORT   EQU      02H      ;INPUT CONTRAST PORT
OCPORT   EQU      02H      ;OUTPUT CONTRAST PORT
IDPORT   EQU      03H      ;INPUT DATA PORT

;**************** END CONSTANTS ************************************

;**************** VARIABLES ****************************************

UDBRT    EQU      0F800H   ;UNSCALED BCD VALUE FOR DESIRED BRIGHTNESS
DBRT     EQU      0F801H   ;8-BIT SCALED VALUE FOR DESIRED BRIGHTNESS
ABRT     EQU      0F802H   ;COMPUTED ACTUAL BRIGHTNESS
BRTOUT   EQU      0F803H   ;BRTNESS-OUT SETTING SENT TO OBPORT
UDCON    EQU      0F810H   ;UNSCALED BCD VALUE FOR DESIRED CONTRAST
DCON     EQU      0F811H   ;8-BIT SCALED VALUE FOR DESIRED CONTRAST
ACON     EQU      0F812H   ;COMPUTED ACTUAL CONTRAST
CONOUT   EQU      0F813H   ;CONTRAST-OUT SETTING SENT TO OCPORT
```

```
OSTAT    EQU      0F820H   ;LOCATION OF OUTPUT STATUS BYTE
ISTAT    EQU      0F821H   ;LOCATION OF INPUT STATUS BYTE
BMAX     EQU      0F830H   ;MAXIMUM SAMPLE VALUE
BMIN     EQU      0F831H   ;MINIMUM SAMPLE VALUE
SUM      EQU      0F832H   ;SUM STORAGE AREA OF 128 SAMPLES (2 BYTES)
TABLE    EQU      0F900H   ;BEGINNING OF 512-BYTE RETICON DATA TBL
STVAL    EQU      0F9C0H   ;BEGINNING OF 128 SAMPLES OF INTEREST

;**************** END VARIABLES ************************************
```

```
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *      INITIALIZATION ROUTINE  - 30 JAN 83                              *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *                                                                       *
;  *  THIS ROUTINE CLEARS ALL RAM WORK AREAS.  THEN THE ROUTINE            *
;  *  INITIALIZES THE CONTROLLER BY STROBING OUTPUT STATUS BITS            *
;  *  ON AND OFF.  THIS PRESETS THE DESIRED BRIGHTNESS AND                 *
;  *  CONTRAST COUNTERS AND CLEARS THE FLAG-GENERATING CIRCUITS.           *
;  *  BIT 3 OF THE OSPORT IS NOT TOGGLED, HOWEVER, UNTIL THE               *
;  *  PROCESSOR IS READY TO READ A RETICON SCAN.  IN ADDITION,             *
;  *  DESIRED BRIGHTNESS AND CONTRAST VALUES ARE INITIALIZED TO            *
;  *  THE VALUES SPECIFIED BY SWITCHES S5 AND S6.                          *
;  *                                                                       *
;  *  INPUTS:  NONE                                                        *
;  *                                                                       *
;  *  OUTPUTS: STACK POINTER IS INITIALIZED                                *
;  *           RAM WORK AREAS ARE CLEARED                                  *
;  *           OSPORT BITS ARE TOGGLED ON AND OFF                          *
;  *           DBRT, DCON ARE INITIALIZED                                  *
;  *                                                                       *
;  *  ROUTINES CALLED:  CLRMEM, BUPDAT, CUPDAT                             *
;  *                                                                       *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

        ORG     0000H

INIT:   LD      SP,STACK        ;INITIALIZE STACK POINTER

        LD      HL,SCRTCH       ;CLEAR SCRATCHPAD WORK AREA
        LD      BC,0300H        ;   AND RETICON DATA TABLE
        CALL    CLRMEM

        LD      A,0FFH          ;TOGGLE OUTPUT STATUS BITS
        OUT     (OSPORT),A      ;   ON AND OFF.  (DON'T TOGGLE
        LD      A,008H          ;   BIT 3 TILL READY TO READ
        OUT     (OSPORT),A      ;   RETICON ARRAY)
        LD      (OSTAT),A       ;SAVE OUTPUT STATUS

        CALL    BUPDAT          ;INITIALIZE DESIRED BRIGHTNESS
        CALL    CUPDAT          ;INITIALIZE DESIRED CONTRAST

        JP      EXEC
```

```
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *      CLEAR MEMORY ROUTINE  - 26 JAN 83                                *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *                                                                       *
;  *  THIS ROUTINE CLEARS A BLOCK OF MEMORY.  THE ROUTINE WAS              *
;  *  TAKEN FROM WADSORTH (REF 13:90).                                     *
;  *                                                                       *
;  *  INPUTS:  STARTING ADDRESS OF BLOCK TO CLEAR IN HL                    *
;  *           NUMBER OF BYTES TO CLEAR IN BC                              *
;  *                                                                       *
;  *  OUTPUTS: CLEARS MEMORY BLOCK ADDRESSED BY HL                         *
;  *                                                                       *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

          ORG     0030H

CLRMEM:   LD      (HL),00H        ;CLEAR MEMORY LOCATION
          CPI                     ;DEC COUNTER, INC HL POINTER
          RET     PO              ;EXIT IF COUNTER ZERO
          JR      CLRMEM          ;ELSE GO CLEAR NEXT BYTE
```

```
;*********************************************************
;*     EXECUTIVE ROUTINE  - 26 JAN 83                    *
;*********************************************************
;*                                                       *
;*  THIS IS THE MAIN PROGRAM.  ONCE ENTERED, THIS ROUTINE *
;*  REPEATS ENDLESSLY, CALLING THE OTHER ROUTINES IN THE  *
;*  PROPER ORDER.  THESE ROUTINES ARE DESCRIBED BELOW.    *
;*                                                       *
;*  INPUTS:  NONE                                        *
;*                                                       *
;*  OUTPUTS: SEE INDIVIDUAL ROUTINES BELOW               *
;*                                                       *
;*  ROUTINES CALLED:  STEST, SCAN, AVGBRT, CNTRST, BADJ, CADJ *
;*                                                       *
;*********************************************************

        ORG     0040H

EXEC:   CALL    STEST           ;UPDATE DESIRED BRT & CON

        CALL    SCAN            ;READ RETICON SCAN

        CALL    AVGBRT          ;COMPUTE AVERAGE BRIGHTNESS

        CALL    CNTRST          ;COMPUTE OVERALL CONTRAST

        CALL    BADJ            ;CORRECT BRIGHTNESS

        CALL    CADJ            ;CORRECT CONTRAST

        JR      EXEC            ;LOOP FOREVER
```

```
;*********************************************************
;*     STATUS UPDATE ROUTINE   - 25 JAN 83               *
;*********************************************************
;*                                                       *
;*  THIS ROUTINE TESTS TO SEE IF THE USER WISHES TO UPDATE *
;*  DESIRED BRIGHTNESS OR CONTRAST VALUES.  IF DESIRED   *
;*  BRIGHTNESS IS TO BE UPDATED, BUPDAT IS CALLED.  IF   *
;*  DESIRED CONTRAST IS TO BE UPDATED, CUPDAT IS CALLED. *
;*                                                       *
;*  INPUTS:  INPUT STATUS PORT IS READ                   *
;*                                                       *
;*  OUTPUTS: DBRT AND DCON ARE UPDATED, IF UPDATES NEEDED *
;*                                                       *
;*  ROUTINES CALLED:  BUPDAT, CUPDAT                     *
;*                                                       *
;*********************************************************

        ORG     0060H

STEST:  PUSH    AF              ;SAVE REGISTER CONTENTS

        IN      A,(ISPORT)      ;CHECK INPUT STATUS BYTE
        LD      (ISTAT),A       ;SAVE IT
        BIT     BBIT,A          ;IF BRIGHTNESS UPDATE REQUESTED,
        CALL    NZ,BUPDAT       ;    ...DO IT

        LD      A,(ISTAT)       ;RECALL INPUT STATUS BYTE
        BIT     CBIT,A          ;IF CONTRAST UPDATE REQUESTED,
        CALL    NZ,CUPDAT       ;    ...DO IT

        POP     AF              ;RESTORE REGISTERS
        RET                     ;RETURN
```

```
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *      BRIGHTNESS UPDATE ROUTINE  - 30 JAN 83                           *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *                                                                       *
;  *  THIS ROUTINE UPDATES THE VALUE FOR DESIRED BRIGHTNESS.               *
;  *  FIRST, THE NEW UNSCALED VALUE FOR DESIRED BRIGHTNESS,                *
;  *  UDBRT, IS READ FROM THE IBPORT (INPUT BRIGHTNESS PORT)               *
;  *  AND SAVED.  THIS VALUE IS THEN CONVERTED TO A SCALED                 *
;  *  BINARY VALUE AND SAVED (DBRT = 256 X UDBRT / DBSF).                  *
;  *  FINALLY, THE ROUTINE TOGGLES BIT 0 OF THE OSPORT ON AND              *
;  *  OFF TO SIGNAL THAT BRIGHTNESS HAS BEEN UPDATED.                      *
;  *                                                                       *
;  *  INPUTS:  IBPORT IS READ                                              *
;  *                                                                       *
;  *  OUTPUTS: UDBRT AND DBRT ARE UPDATED                                  *
;  *           BIT 0 OF OSPORT IS TOGGLED ON AND OFF                       *
;  *                                                                       *
;  *  ROUTINES CALLED:  CONVRT, DIVIDE                                     *
;  *                                                                       *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

        ORG     0080H

BUPDAT: PUSH    AF              ;SAVE REGISTER CONTENTS
        PUSH    HL
        PUSH    BC

        IN      A,(IBPORT)      ;INPUT NEW VALUE FOR UNSCALED
        LD      (UDBRT),A       ;   DESIRED BRIGHTNESS & SAVE IT
        CALL    CONVRT          ;CONVERT IT TO A BINARY VALUE
        LD      H,A             ;LOAD (256 X UDBRT) INTO HL
        LD      L,00H
        LD      C,DBSF          ;LOAD BRTNESS SCALE FACTOR IN C
        CALL    DIVIDE          ;CALC DBRT = 256 X UDBRT / DBSF
        LD      A,L             ;SAVE RESULT
        LD      (DBRT),A

        LD      A,(OSTAT)       ;TOGGLE BUPDAT ACKNOWLEDGE BIT
        SET     BBIT,A          ;   ... ON ...
        OUT     (OSPORT),A
        RES     BBIT,A          ;   ... THEN OFF
        OUT     (OSPORT),A

        POP     BC              ;RESTORE REGISTERS
        POP     HL
        POP     AF
        RET                     ;RETURN
```

```
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *     CONTRAST UPDATE ROUTINE  - 30 JAN 83                              *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *                                                                       *
;  *  THIS ROUTINE UPDATES THE VALUE FOR DESIRED CONTRAST.                 *
;  *  FIRST, THE NEW UNSCALED VALUE FOR DESIRED CONTRAST,                  *
;  *  UDCON, IS READ FROM THE ICPORT (INPUT CONTRAST PORT)                 *
;  *  AND SAVED.  THIS VALUE IS THEN CONVERTED TO A SCALED                 *
;  *  BINARY VALUE AND SAVED (DCON = 256 X UDCON / DCSF).                  *
;  *  FINALLY, THE ROUTINE TOGGLES BIT 1 OF THE OSPORT ON AND              *
;  *  OFF TO SIGNAL THAT CONTRAST HAS BEEN UPDATED.                        *
;  *                                                                       *
;  *  INPUTS:  ICPORT IS READ                                              *
;  *                                                                       *
;  *  OUTPUTS: UDCON AND DCON ARE UPDATED                                  *
;  *           BIT 1 OF OSPORT IS TOGGLED ON AND OFF                       *
;  *                                                                       *
;  *  ROUTINES CALLED:  CONVRT, DIVIDE                                     *
;  *                                                                       *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

        ORG     00B0H

CUPDAT: PUSH    AF              ;SAVE REGISTER CONTENTS
        PUSH    HL
        PUSH    BC

        IN      A,(ICPORT)      ;INPUT NEW VALUE FOR UNSCALED
        LD      (UDCON),A       ;   DESIRED CONTRAST & SAVE IT
        CALL    CONVRT          ;CONVERT IT TO A BINARY VALUE
        LD      H,A             ;LOAD (256 X UDCON) INTO HL
        LD      L,00H
        LD      C,DCSF          ;LOAD CONTRAST SCALE FACTOR IN C
        CALL    DIVIDE          ;CALC DCON = 256 X UDCON / DCSF
        LD      A,L             ;SAVE RESULT
        LD      (DCON),A

        LD      A,(OSTAT)       ;TOGGLE CUPDAT ACKNOWLEDGE BIT
        SET     CBIT,A          ;   ... ON ...
        OUT     (OSPORT),A
        RES     CBIT,A          ;   ... THEN OFF
        OUT     (OSPORT),A

        POP     BC              ;RESTORE REGISTERS
        POP     HL
        POP     AF
        RET                     ;RETURN
```

```
; * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
; *      DECIMAL TO BINARY CONVERSION ROUTINE     - 30 JAN 83          *
; * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
; *                                                                     *
; *  THIS ROUTINE CONVERTS AN 8-BIT BINARY-CODED DECIMAL                *
; *  (BCD) NUMBER TO ITS BINARY EQUIVALENT                              *
; *                                                                     *
; *  INPUTS:  8-BIT BCD NUMBER IN A                                     *
; *                                                                     *
; *  OUTPUTS: 8-BIT BINARY EQUIVALENT IN A                              *
; *                                                                     *
; *  REGISTERS AFFECTED:  A                                             *
; *                                                                     *
; * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

        ORG     0100H

CONVRT: PUSH    DE              ;SAVE REGISTER CONTENTS
        PUSH    AF

        LD      E,A             ;SAVE THE BCD NUMBER IN E
        AND     0F0H            ;STRIP OFF DIGIT2 & CLEAR C BIT
        RRA                     ;A = 8 X D1
        LD      D,A             ;SAVE 8 X D1
        RRA                     ;A = 4 X D1
        RRA                     ;A = 2 X D1
        ADD     A,D             ;A = 10 X D1
        LD      D,A             ;SAVE 10 X D1

        LD      A,E             ;GET DIGIT2 OF BCD NUMBER
        AND     0FH             ;STRIP OFF DIGIT1
        ADD     A,D             ;A = (10 X D1) + D2
        LD      D,A             ;SAVE RESULT

        POP     AF              ;RESTORE F REGISTER
        LD      A,D             ;LEAVE BINARY VALUE IN A
        POP     DE              ;RESTORE DE
        RET                     ;RETURN
```

```
;*********************************************
;*     DIVIDE ROUTINE  - 29 JAN 83           *
;*********************************************
;*                                           *
;*  THIS ROUTINE DIVIDES A 16-BIT UNSIGNED DIVIDEND IN HL BY  *
;*  AN 8-BIT UNSIGNED DIVISOR IN C TO YIELD AN 8-BIT QUOTIENT *
;*  (WITH LSB ROUNDED) IN L.  THE REMAINDER THAT EXISTED      *
;*  BEFORE ROUNDING IS LEFT IN H.                             *
;*                                                            *
;*  INPUTS:  16-BIT DIVIDEND (DVD) IN HL                      *
;*           8-BIT DIVISOR (DVS) IN C                         *
;*                                                            *
;*  OUTPUTS: 8-BIT ROUNDED QUOTIENT (QUO) IN L                *
;*           8-BIT REMAINDER (BEFORE ROUNDING) IN H           *
;*                                                            *
;*  REG'S AFFECTED: HL                                        *
;*                                                            *
;*********************************************

        ORG     0120H

DIVIDE: PUSH    AF              ;SAVE REGISTER CONTENTS
        PUSH    BC
        LD      B,08H           ;INITIALIZE COUNTER FOR 8 PASSES

DVLOOP: ADD     HL,HL           ;SHIFT DVD & QUO LEFT 1 BIT
        JR      C,OVRFLW        ;JUMP IF DVD OVERFLOWED
        LD      A,H
        SUB     C               ;CAN DVD BE DIVIDED?
        JR      C,DUNTST        ;IF NO, GO TO NEXT STEP
        LD      H,A             ;IF YES, DVD - DVS
        INC     L               ;SET LSB OF QUO
DUNTST: DJNZ    DVLOOP          ;LOOP UNTIL CTR = 0
        JR      ROUND           ;GO ROUND RESULT IF DONE

OVRFLW: LD      A,H             ;GET DVD
        SUB     C               ;DVD - DVS
        LD      H,A             ;SAVE RESULT IN DVD
        INC     L               ;SET LSB OF QUO
        DJNZ    DVLOOP          ;LOOP UNTIL CTR = 0

ROUND:  AND     A               ;CLEAR CARRY BIT
        LD      A,C             ;DIVIDE DVS BY 2
        RRA
        CP      H               ;COMPARE REM WITH 1/2 DVS
        JR      NC,DVEND        ;IF REM < 1/2 DVS, RETURN
        INC     L               ;ELSE ROUND QUO UP 1 BIT
DVEND:  POP     BC              ;RESTORE REGISTERS
        POP     AF
        RET                     ;RETURN
```

```
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *      SCAN ROUTINE     -  25 JAN 83                                    *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *                                                                       *
;  *  THIS ROUTINE READS 512 BYTES OF DATA FROM PORT 3.  DATA             *
;  *  IS READ AS QUICKLY AS POSSIBLE, WITH NO WAITING FOR                 *
;  *  HANDSHAKES.  IT IS ASSUMED THAT THE EXTERNAL HARDWARE               *
;  *  RUNS SLOWER THAN THIS ROUTINE, AND INSERTS WAIT STATES              *
;  *  TO SYNCHRONIZE THE COMPUTER WITH THE OTHER HARDWARE.                *
;  *                                                                      *
;  *  INPUTS:  INPUT PORT 3 IS READ                                       *
;  *                                                                      *
;  *  OUTPUTS: 512-BYTE RETICON DATA TABLE IS UPDATED                     *
;  *           WTBIT OF OUTPUT STATUS PORT IS TOGGLED OFF & ON            *
;  *                                                                      *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

        ORG     0160H

SCAN:   PUSH    AF              ;SAVE REGISTER CONTENTS
        PUSH    HL
        PUSH    BC

        LD      A,(OSTAT)       ;RESET WAIT STATE CONTROLLER
        RES     WTBIT,A         ;   BY TOGGLING RESET BIT OFF ...
        OUT     (OSPORT),A
        SET     WTBIT,A         ; ... THEN ON AGAIN.
        OUT     (OSPORT),A

        LD      C,IDPORT        ;AIM C AT INPUT DATA PORT
        LD      HL,TABLE        ;AIM HL AT START OF TABLE
        LD      B,00H           ;SET B AS A 256-BYTE COUNTER

        INIR                    ;READ 256 BYTES
        INIR                    ;READ NEXT 256 BYTES

        POP     BC              ;RESTORE REGISTERS
        POP     HL
        POP     AF
        RET                     ;RETURN
```

```
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *      BRIGHTNESS CALCULATION ROUTINE  -  29 AUG 83                     *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *                                                                       *
;  *  THIS ROUTINE COMPUTES AVERAGE BRIGHTNESS MEASURED BY THE             *
;  *  RETICON ARRAY.  128 VALUES ARE USED FOR THE BRIGHTNESS               *
;  *  CALCULATION.  THIS REPRESENTS THE MIDDLE PORTION OF THE              *
;  *  512 ARRAY WHICH IS OF INTEREST (192,128,192).                        *
;  *  SUMVAL IS USED TO SUM THE VALUES OF INTEREST.                        *
;  *                                                                       *
;  *  INPUTS:  RETICON DATA                                                *
;  *                                                                       *
;  *  OUTPUTS: ABRT (ACTUAL BRIGHTNESS) IS UPDATED                         *
;  *                                                                       *
;  *  ROUTINES CALLED:  SUMVAL                                             *
;  *                                                                       *
;  *  MEMORY LOCNS AFFECTED:  ABRT, SUM                                    *
;  *                                                                       *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

        ORG     0190H

AVGBRT: PUSH    AF              ;SAVE REGISTER CONTENTS
        PUSH    HL

        CALL    SUMVAL          ;SUM THE 128 VALUES OF INTEREST

        LD      HL,(SUM)        ;ROUND 8 MOST SIGNIFICANT BITS

        ADD     HL,HL           ;DIVIDE SUM BY 128

        BIT     7,L             ;ROUND RESULT
        JR      Z,SAVE          ;IF BIT 7 NOT SET, SKIP AHEAD
        INC     H               ;IF BIT 7 SET, ROUND UP

 SAVE:  LD      A,H             ;MOVE MOST SIGNIFICANT 8 BITS INTO A
        LD      (ABRT),A        ;   AND SAVE RESULT IN ABRT

        POP     HL              ;RESTORE REGISTERS
        POP     AF
        RET                     ;RETURN
```

```
;*****************************************************************
;*                SUMMING ROUTINE  -  30 AUG 83                  *
;*****************************************************************
;*                                                               *
;*  THIS ROUTINE SUMS THE 128 BYTES OF INTEREST OF THE MIDDLE    *
;*  PORTION OF THE DATA TABLE.  THIS 128 BYTE PORTION BEGINS     *
;*  AT ADDRESS 0F9C0H AND CONTINUES THROUGH 0FA3FH.  THE SUM     *
;*  IS STORED IN TWO (2) SEQUENTIAL MEMORY LOCATIONS ADDRESSED   *
;*  BY SUM, WITH THE LSB IN THE FIRST BYTE.                      *
;*                                                               *
;*  INPUTS:  RETICON DATA                                        *
;*                                                               *
;*  OUTPUTS: SUM IS UPDATED (SUM OF MIDDLE 128 DATA SAMPLES)     *
;*                                                               *
;*  ROUTINES CALLED:  NONE                                       *
;*                                                               *
;*  MEMORY LOCNS AFFECTED:  SUM (2 BYTES)                        *
;*                                                               *
;*****************************************************************

        ORG     01B0H

SUMVAL: PUSH    AF              ;SAVE REGISTER CONTENTS
        PUSH    HL
        PUSH    DE
        PUSH    BC

        LD      DE,STVAL        ;AIM DE AT BEGINNING OF START VALUE
        LD      BC,080H         ;SET COUNTER FOR 128 SAMPLES
        LD      HL,00H          ;  AND INITIALIZE START TO 0

  NEXT: LD      A,(DE)          ;PUT FIRST VALUE INTO A
        INC     DE              ;INCREMENT COUNTER
        ADD     A,L             ;ADD VALUE TO PREVIOUS SUM
        LD      L,A             ;MOVE SUM INTO L
        JR      NC,TEST         ;CHECK CARRY STATUS
        INC     H               ;INCREMENT ADDRESS POINTER

  TEST: DEC     C               ;DECREMENT 1 FROM TOTAL TO BE SUMMED
        JR      NZ,NEXT         ;CHECK TO SEE IF COUNTER IS FINISHED

        LD      (SUM),HL        ;SAVE RESULT IN SUM

        POP     BC              ;RESTORE REGISTERS
        POP     DE
        POP     HL
        POP     AF
        RET                     ;RETURN
```

```
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *      ACTUAL CONTRAST ROUTINE  - 30 JAN 83                             *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *                                                                       *
;  *  THIS ROUTINE COMPUTES ACTUAL CONTRAST FROM THE RETICON               *
;  *  DATA.  THE ALGORITHM USED IS:                                        *
;  *              ACON = 256 X (BMAX - BMIN) / (BMAX + BMIN)               *
;  *                   = 256 X (BMAX - BMIN) / (2 X BAVG)                  *
;  *  NOTE:  ACON IS ACTUALLY SCALED (MULTIPLIED BY 256)                   *
;  *         SINCE TRUE ACON WOULD BE A FRACTION.                          *
;  *                                                                       *
;  *  INPUTS:  ABRT (= BAVG), RETICON DATA                                 *
;  *                                                                       *
;  *  OUTPUTS: ACON, BMAX, BMIN ARE UPDATED                                *
;  *                                                                       *
;  *  ROUTINES CALLED:  FMAX, FMIN, DIVIDE                                 *
;  *                                                                       *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

        ORG     0200H

CNTRST: PUSH    AF              ;SAVE REGISTER CONTENTS
        PUSH    HL
        PUSH    BC

        CALL    FMAX            ;FIND MAX BRIGHTNESS VALUE
        CALL    FMIN            ;FIND MIN BRIGHTNESS VALUE
        LD      A,(BMIN)        ;LOAD MIN BRIGHTNESS
        LD      B,A
        LD      A,(BMAX)        ;LOAD MAX      "
        SUB     B               ;BMAX - BMIN
        LD      H,A             ;PUT DIVIDEND OF
        LD      L,00H           ;    256 X (BMAX - BMIN) IN HL
        LD      A,(ABRT)        ;PUT DIVISOR OF
        LD      C,A             ;    ABRT (= BAVG) IN C
        CALL    DIVIDE          ;COMPUTE 256 X (BMAX-BMIN)/ABRT
        AND     A               ;CLEAR CARRY BIT
        LD      A,L             ;NOW COMPUTE
        RRA                     ;    256 X (BMAX-BMIN)/(2 X ABRT)
        LD      (ACON),A        ;SAVE RESULT

        POP     BC              ;RESTORE REGISTERS
        POP     HL
        POP     AF
        RET                     ;RETURN
```

```
;*********************************************************
;*     FIND MAX ROUTINE  - 29 AUG 83                     *
;*********************************************************
;*                                                       *
;*  THIS ROUTINE FINDS THE MAX VALUE IN THE RETICON DATA TABLE *
;*  OF VALUES OF INTEREST (128 VALUES).                  *
;*                                                       *
;*  INPUTS:  RETICON DATA                                *
;*                                                       *
;*  OUTPUTS: BMAX IS UPDATED                             *
;*                                                       *
;*********************************************************

        ORG     0230H

FMAX:   PUSH    AF              ;SAVE REGISTER CONTENTS
        PUSH    HL
        PUSH    BC
        PUSH    DE

        LD      HL,STVAL        ;AIM TABLE POINTER AT FIRST
                                ;   SAMPLE OF INTEREST

        LD      DE,80H          ;PLACE 128D INTO DE

        LD      A,(HL)          ;SAVE 1ST VALUE AS MAX
        INC     HL              ;INCREMENT POINTER
LOOP1:  CP      (HL)            ;COMPARE NEXT VALUE
        JR      NC,DCNT1        ;IF NOT LARGER, SKIP AHEAD
        LD      A,(HL)          ;IF LARGER, SAVE NEW MAX
DCNT1:  INC     HL              ;INCREMENT POINTER
        DEC     E               ;DECREMENT COUNTER
        JR      NZ,LOOP1        ;LOOP TILL DONE

        LD      (BMAX),A        ;SAVE FINAL BMAX VALUE

        POP     DE              ;RESTORE REGISTERS
        POP     BC
        POP     HL
        POP     AF
        RET                     ;RETURN
```

```
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *      FIND MIN ROUTINE  - 29 AUG 83                                  *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;  *                                                                     *
;  *  THIS ROUTINE FINDS THE MIN VALUE IN THE RETICON DATA TABLE         *
;  *  OF VALUES OF INTEREST (128 VALUES).                                *
;  *                                                                     *
;  *  INPUTS:  RETICON DATA                                              *
;  *                                                                     *
;  *  OUTPUTS: BMIN IS UPDATED                                           *
;  *                                                                     *
;  * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

          ORG     0260H

FMIN:     PUSH    AF              ;SAVE REGISTER CONTENTS
          PUSH    HL
          PUSH    BC
          PUSH    DE

          LD      HL,STVAL        ;AIM TABLE POINTER AT FIRST
                                  ;   SAMPLE OF INTEREST
          LD      DE,80H          ;LOAD 128D INTO DE

          LD      A,(HL)          ;SAVE 1ST VALUE AS MIN
          INC     HL              ;INCREMENT POINTER
LOOP2:    CP      (HL)            ;COMPARE NEXT VALUE
          JR      C,DCNT2         ;IF LARGER, SKIP AHEAD
          LD      A,(HL)          ;   ELSE, SAVE NEW MIN
DCNT2:    INC     HL              ;INCREMENT POINTER
          DEC     E               ;DECREMENT COUNTER
          JR      NZ,LOOP2        ;LOOP TILL DONE

          LD      (BMIN),A        ;SAVE FINAL BMIN VALUE

          POP     DE              ;RESTORE REGISTERS
          POP     BC
          POP     HL
          POP     AF
          RET                     ;RETURN
```

```
;* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;*      BRIGHTNESS ADJUST ROUTINE  - 30 JAN 83                           *
;* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *
;*                                                                       *
;*  THIS ROUTINE SENDS BRIGHTNESS CORRECTIONS WHEN                       *
;*  DBRT AND ABRT DIFFER.                                                *
;*                                                                       *
;*  INPUTS:  DBRT, ABRT, BRTOUT                                          *
;*                                                                       *
;*  OUTPUTS: BRTOUT IS UPDATED                                           *
;*                                                                       *
;* * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * * *

        ORG     0290H

BADJ:   PUSH    AF
        PUSH    BC

        LD      C,OBPORT        ;AIM C AT OUTPUT BRTNSS PORT
        LD      A,(ABRT)        ;LOAD ACTUAL BRIGHTNESS
        LD      B,A
        LD      A,(DBRT)        ;LOAD DESIRED BRIGHTNESS
        SUB     B               ;DBRT - ABRT
        JR      Z,BEXIT         ;DO NOTHING IF THEY MATCH
        LD      A,(BRTOUT)      ;LOAD OLD BRTOUT VALUE
        JR      C,BHI           ;SKIP AHEAD IF ABRT IS TOO HI

BLO:    INC     A               ;KICK OLD BRTOUT UP A TICK
        JR      BOUT            ;SKIP AHEAD

BHI:    DEC     A               ;DROP OLD BRTOUT DOWN A TICK

BOUT:   OUT     (C),A           ;OUTPUT CORRECTED VALUE
        LD      (BRTOUT),A      ;    AND SAVE IT

BEXIT:  POP     BC
        POP     AF
        RET                     ;RETURN
```

```
;*********************************************************
;*     CONTRAST ADJUST ROUTINE  - 30 JAN 83              *
;*********************************************************
;*                                                       *
;*  THIS ROUTINE SENDS CONTRAST CORRECTIONS WHEN         *
;*  DCON AND ACON DIFFER.                                *
;*                                                       *
;*  INPUTS:  DCON, ACON, CONOUT                          *
;*                                                       *
;*  OUTPUTS: CONOUT IS UPDATED                           *
;*                                                       *
;*********************************************************

        ORG     02C0H

CADJ:   PUSH    AF
        PUSH    BC

        LD      C,OCPORT        ;AIM C AT OUTPUT CONTRAST PORT
        LD      A,(ACON)        ;LOAD ACTUAL CONTRAST
        LD      B,A
        LD      A,(DCON)        ;LOAD DESIRED CONTRAST
        SUB     B               ;DCON - ACON
        JR      Z,CEXIT         ;DO NOTHING IF THEY MATCH
        LD      A,(CONOUT)      ;LOAD OLD CONOUT VALUE
        JR      C,CHI           ;SKIP AHEAD IF ACON IS TOO HI

CLO:    INC     A               ;KICK OLD CONOUT UP A TICK
        JR      COUT            ;SKIP AHEAD

CHI:    DEC     A               ;DROP OLD CONOUT DOWN A TICK

COUT:   OUT     (C),A           ;OUTPUT CORRECTED VALUE
        LD      (CONOUT),A      ;   AND SAVE IT

CEXIT:  POP     BC
        POP     AF
        RET                     ;RETURN

        END
```

VITA

Mark H. Swann was born on 23 July 1952 in Springfield, Tennessee. He graduated from Springfield High School in 1970 and attended Tennessee Technological University from which he recieved the degree of Bachelor of Science in Electrical Engineering in June 1975. Upon graduation, he was employed as an electronic engineer with the Airborne Electronics Division, Directorate of Maintenance, Warner Robins Air Logistics Center, Robins Air Force Base, Georgia. He worked here in the Automatic Test Equipement, Software Support Center Branch until entering the School of Engineering, Air Force Institute of Technology, in June 1982.

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Title: An Automatic Sine-Wave Grating Controller To Be Used For Contrast Sensitivity Testing

Abstract: This report documents the additional design, construction, and testing of a brightness and contrast controller system which includes an embedded microcomputer. It is planned that researchers will use this controller to maintain prescribed video output of laboratory video monitors during vision research.
The controller requires a video signal consisting of a sine-wave grating. A 512-element photodiode array directly measures the monitor's screen to produce an analog signal which is then digitized and stored in the computer. These data are used to compute the actual

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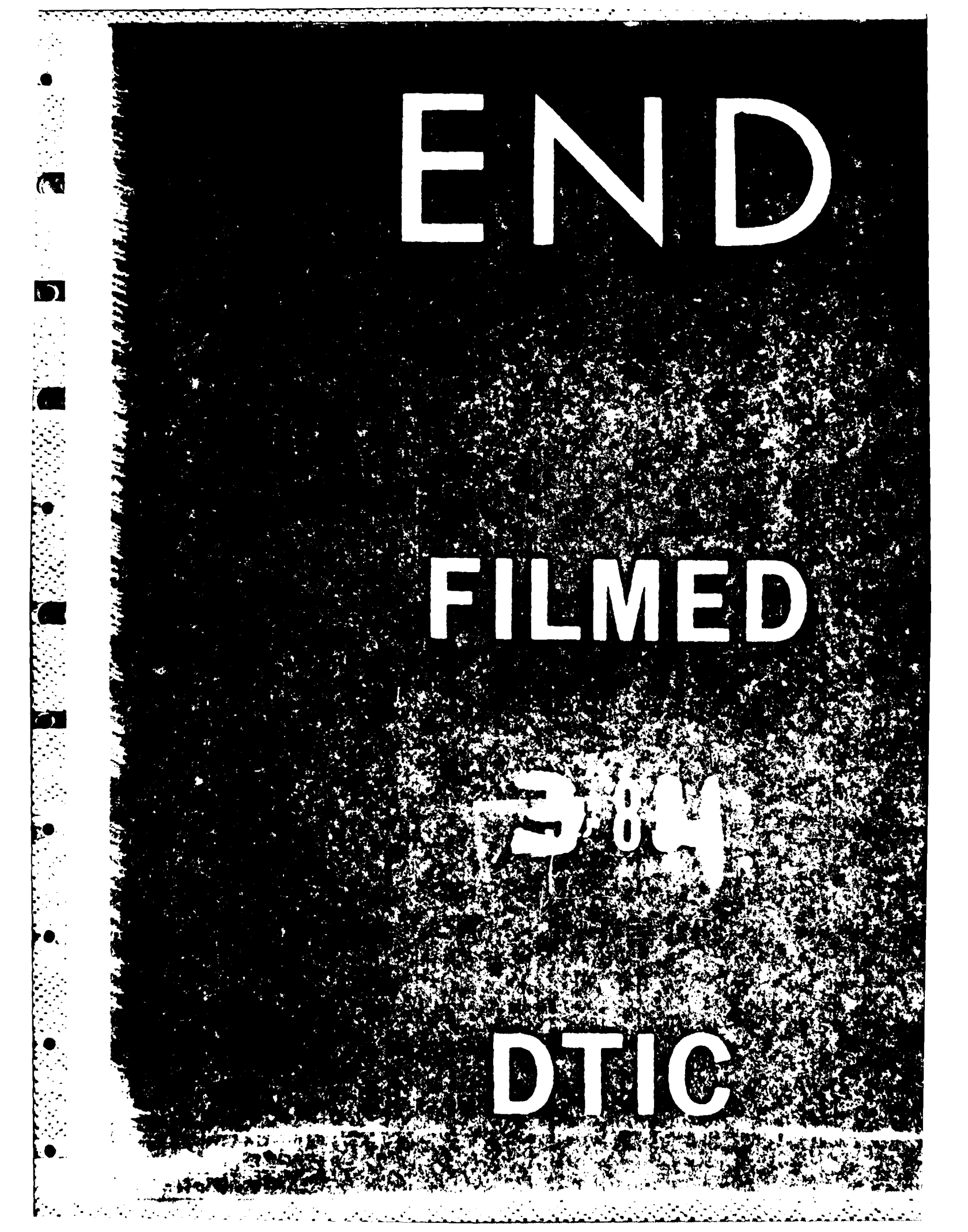
brightness and contrast of the monitor. Correction values are sent to the brightness and contrast control circuits when the desired and measured values differ.

In an attempt to complete the controller's system requirements, the controller prototype hardware was completed and partially packaged. Closed-loop system testing was performed for both the brightness and contrast control circuitry. Brightness and contrast control circuitry, a vertical synch pulse generator, a user-interface console, and power supply with additional voltage-regulator circuitry were designed and added to the existing prototype. Existing software was tested and modified to allow the controller to operate more accurately. Final packaging, along with additional system testing, must be accomplished for the controller to be a finished product.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